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STUDY OF THE PHYSICS OF INSULATING FILMS AS RELATED TO THE RELIABILITY OF METAL-OXIDE SEMICONDUCTOR (MOS) DEVICES

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This report covers a discussion of high current injection into wide bandgap insulators, the use of Si-rich SiO_2 in DEIS EAROM FET's, modeling calculations for predicting the operation of DEIS EAROM's, the relationship of electron traps in SiO_2 to OH groups and H_2O, the physics of very thin (50-200 Å) gate insulators, the relationship of interface state generation to electron capture on trapped holes near the Si-SiO_2 interface, radiation damage of SiO_2 layers exposed to plasmas, the effect of annealing on the Al-SiO_2 interfacial energy barrier, and a technique for measuring the diffusion of an oxidant in SiO_2 films.

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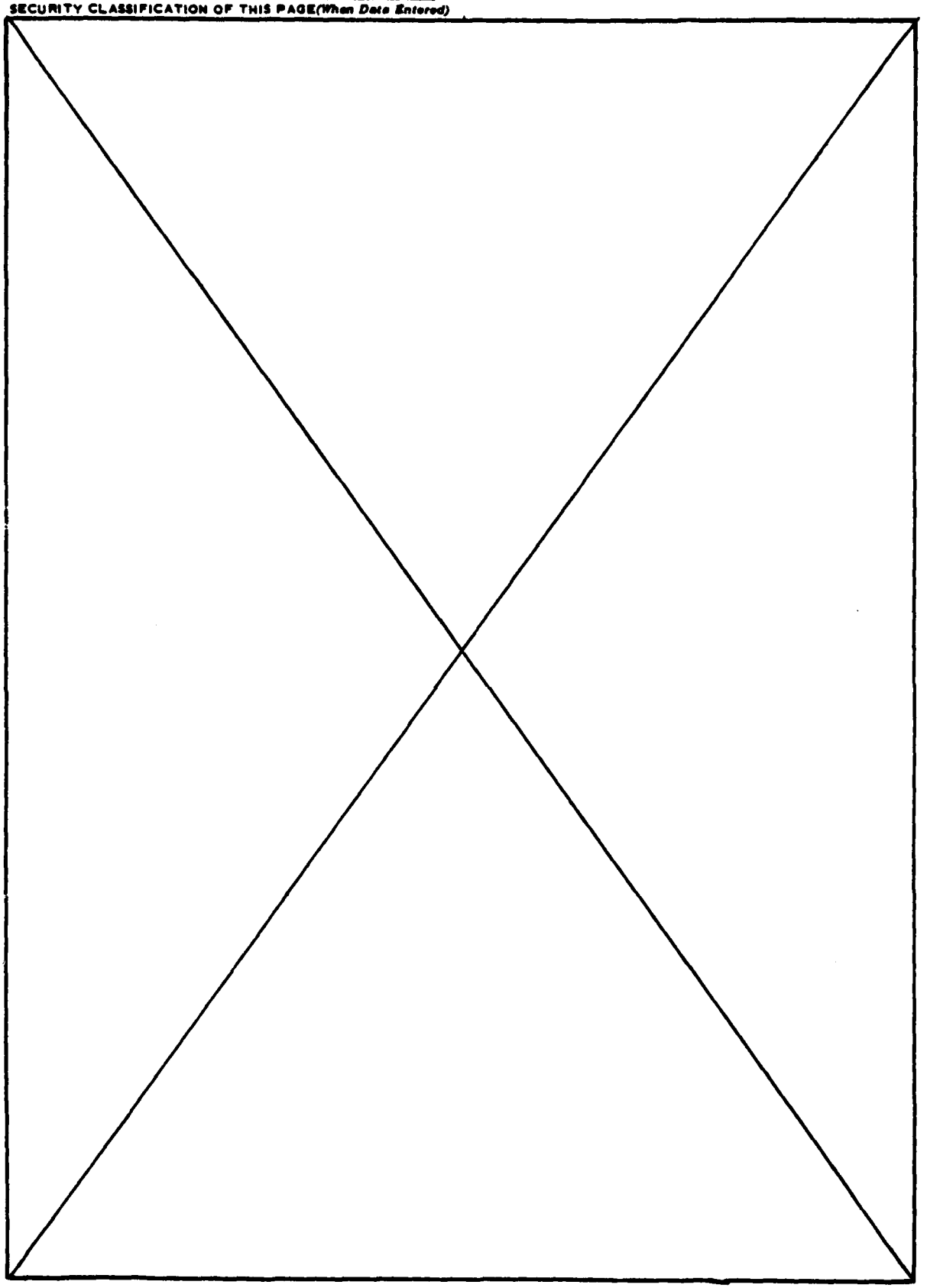

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INTRODUCTION

The importance of SiO_2 and other insulators, in particular Si-rich SiO_2, in electronic devices, such as non-volatile memories is currently being demonstrated in both military and commercial applications. This report blends basic studies on SiO_2 and Si-rich SiO_2 films, such as insulator trapping, SiO_2 growth kinetics, radiation damage effects, and contact-insulator interface effects, with applications using these physical phenomena that are observed. In particular, our development of a new type of non-volatile memory using stacked layers of Si-rich SiO_2 and SiO_2 is discussed in detail.

Si-rich SiO_2 layers, when deposited on top of thermal SiO_2, have been shown to give high electronic current injection into the SiO_2 layer at moderate average electric fields. This phenomenon is believed to be associated with the Si-rich SiO_2–SiO_2 interface and the two phase nature of the Si-rich SiO_2 material. This and related phenomena where surface roughness or graded band-gap insulating layers are used to achieve high current injection are discussed in the paper entitled "Charge Injection into Wide Energy Band-Gap Insulators" by D.J. DiMaria. Two other papers entitled "Electrically-Alterable Read-Only-Memory Using Si-rich SiO_2 Injectors and a Floating Polycrystalline Silicon Storage Layer" by D.J. DiMaria, K.M. DeMeyer, C.M. Serrano, and D.W. Dong, and "Dual-Electron-Injector-Structure Electrically-Alterable Read-Only-Memory Modeling Studies" by D.J. DiMaria, K.M. DeMeyer, and D.W. Dong discuss the applications of using a stacked layer of Si-rich SiO_2, SiO_2, and Si-rich SiO_2 in electrically-alterable read-only-memories (EAROM's). This stacked layer called a dual-electron-injector-structure (DEIS) is incorporated in between a degeneratively, phosphorus-doped polycrystalline silicon (poly-Si) control gate and floating gate. Electrons are injected from the top Si-rich SiO_2 injector under negative control gate voltages into the SiO_2 layer at moderate applied electric fields. These injected electrons then flow onto the floating gate electrode. This is called the "write" operation of this memory. To "erase" the floating poly-Si storage layer, electrons are pulled off the floating gate under positive control gate voltages using the enhanced current injection characteristics of the bottom Si-rich SiO_2–SiO_2 interface. The charge state of the DEIS memory is sensed by field-effect-transistor (FET) operation. The modeling paper described a simple physical model based on the current injection characteristics of the two Si-rich SiO_2–SiO_2 interfaces in the DEIS stack and the changing internal fields. This model predicts fairly accurately the operation of

these devices under any write/erase conditions and any device geometrical configuration. As demonstrated in these articles, the cause of degradation in the DEIS EAROM's is electron charge trapping on energetically deep sites in the intervening SiO_2 layer of the DEIS stack.

The next two papers entitled "Identification of Electron Traps in Thermal Silicon Dioxide Films" by A. Hartstein and D.R. Young, and "Very Thin Gate Insulators" by S.K. Lai discuss the identification and means of reducting these electron trapping centers in SiO_2. The paper of Hartstein and Young describes a strong correlation of infrared (IR) absorption data for SiOH groups and H_2O in the bulk of SiO_2 films using the attenuated total reflectance technique (ATR) with trap densities for sites with electronic capture cross-sections of 1×10^{-17} and 2×10^{-18} cm^2, respectively. A discussion of trap reduction using annealing in N_2, Ar, or H_2/N_2 mixtures is discussed in both papers. Lai points out the advantages and disadvantages of very thin SiO_2 layers (50-200 Å in thickness) not only in terms of electron trapping but also in terms of reproducibility, breakdown, reliability, and radiation hardness. Some discussion of thin silicon oxynitride layers as a possible replacement for SiO_2 as the gate insulator in FET's is also presented in Lai's paper.

Radiation damage effects in terms of interface state generation and bulk neutral trap generation are discussed in the papers entitled "Two Carrier Nature of Interface State Generation in Hole Trapping and Radiation Damage" by S.K. Lai, and "Review of RIE Induced Radiation Damage in Silicon Dioxide" by L.M. Ephrath and D.J. DiMaria. In S.K. Lai's paper, the generation of an interface state peaked in energy approximately 0.3 eV below the bottom of the Si conduction band is shown to occur when electrons are captured coulombically on trapped holes near the Si–SiO_2 interface. This interface state peak is speculated to be caused by the formation of an electron-hole dipolar complex rather than by the annihilation of the trapped holes. This peak is believed to be the same one observed in radiation damage of SiO_2 layers where energies greater that the SiO_2 band-gap generate electron-hole pairs in the oxide bulk. In the review paper by L.M. Ephrath and D.J. DiMaria, radiation damage introduced by plasmas during reactive ion etching (RIE) and plasma etching of SiO_2 films is discussed. RIE is a necessary processing tool for achieving small area FET dimensions necessary for very large scale integration (VLSI). This paper also demonstrates that a large reduction in radiation-induced neutral trap density can be obtained when either thick Al or poly-Si gate electrodes shield the underlying gate oxide during RIE to define source and drain contacts during realistic FET processing.

Al contacts to SiO_2 are known to react with the SiO_2 to give good adherence. The Al–SiO_2 interfacial energy barrier height is investigated after different annealing treatments using internal photoemission techniques in the paper entitled "Effect of Forming Gas Anneal on Al–SiO_2 Internal Photoemission Characteristics" by P.M. Solomon and D.J. DiMaria. In this paper, it is shown that the effect of a standard post-metallization forming gas (H_2/N_2 mixture) anneal is to increase the energy barrier height by approximately 0.3 eV and cause a significant departure from a Schottky barrier lowering model.

In the final paper included in this report entitled "Silicon Oxidation Studies: Measurement of the Diffusion of Oxidant in SiO_2 Films", E.A. Irene shows evidence for different dominant modes of oxidation at different oxidation temperatures using a lag-time diffusion method. He uses in-situ ellipsometry to measure the diffusion of the oxidant through a growing SiO_2 film. The technique enables the identification of a non-Fickian transport regime below 900°C and a Fickian regime above 1000°C.

Papers Published:

1. A. Hartstein and D.R. Young, "Identification of Electron Traps in Thermal Silicon Dioxide Films", *Appl. Phys. Lett.* 38, 631 (1981).

2. S.K. Lai, "Very Thin Gate Insulators", in Semiconductor Silicon 1981, edited by H.R. Huff, R.J. Kriegler, and Y. Takeishi (The Electrochemical Society, Inc., N.J., 1981), pp. 416-423.

3. L.M. Ephrath and D.J. DiMaria, "Review of RIE Induced Radiation Damage in Silicon Dioxide", Solid State Technology, p. 188, April 1981.

Presentations Made:

1. A.M. Hartstein, Z.A. Weinberg, and D.J. DiMaria, "Experimental Verification of Quantum Mechanical Image Force Theory" at the March Meeting of the American Physical Society, Phoenix, Arizona, March 16-20, 1981.

2. D.J. DiMaria, K.M. DeMeyer, and D.W. Dong, "Dual-Electron-Injector-Structure Electrically-Alterable Read-Only-Memory Studies" at the 1980 Semiconductor Interface Specialists Conference (SISC) in Ft. Lauderdale, Florida, December 4-6, 1980.

3 S.K. Lai, D.R. Young, and J.A. Calise, "Reduction of Electron Trapping in Oxides" at the 1980 Semiconductor Interface Specialists Conference (SISC) in Ft. Lauderdale, Florida, December 4-6, 1980.

4. A. Hartstein and D.R. Young, "Correlation of Impurities to Electron Traps in SiO_2", 1980 Semiconductor Interface Specialists Conference (SISC), in Ft. Lauderdale, Florida, December 4-6, 1980.

5. D.J. DiMaria, ***(Invited)***, "Charge Injection into Wide Energy Bang-gap Insulators", at Conference on Insulating Films on Semiconductors, University of Erlangen, Federal Republic of Germany, April 27-29, 1981.

6. D.J. DiMaria, "Charge Injection into Wide Energy Band-gap Insulators", at ESAT Laboratory, Catholic University of Leuven, Leuven, Belgium, May 4, 1981.

7. D.J. DiMaria, "Charge Injection into Wide Energy Band-gap Insulators", at University of Aachen, Federal Republic of Germany, April 30, 1981.

8. D.J. DiMaria, "Charge Injection into Wide Energy Band-gap Insulators", at University of Minnesota, Minneapolis, Minnesota, May 11, 1981.

9. S.K. Lai, ***(Invited)*** "Very Thin Gate Insulators", at the Electrochemical Society Meeting, Minneapolis, Minnesota, May 10-15, 1981.

10. S.K. Lai and D.R. Young, "Interface Effects in Avalanche Injection of Electrons into Silicon Dioxide", at Conference on Insulating Films on Semiconductors, University of Erlangen, Federal Republic of Germany, April 27-29, 1981.

11. J.M. Aitken and B.L. Crowder, "Al/Ti as Contact Metallurgy for VLSI Applications Part II - Annealing of Radiation Damage in MOSFET's", at the Electrochemical Society Meeting, Minneapolis, Minnesota, May 10-15, 1981.

12. A. Reisman, J.M. Aitken, A.K. Ray, M. Berkenblit, C.J. Merz and R.P. Havreluk, "Annealing of Gate Insulators at Elevated Pressure", at at the Electrochemical Society Meeting, Minneapolis, Minnesota, May 10-15, 1981.

Charge Injection into Wide Energy Bang-Gap Insulators

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ABSTRACT

Charge injection into wide energy band-gap insulators such as silicon dioxide, which is one of the building blocks of the solid-state industry, is very difficult because of the large energy band-gap of SiO_2 (~ 9 eV) and the large energy barriers (> 2 eV) it forms with contacting metals and semiconductors. High current injection into insulators at moderate to low electric fields can be obtained by modifying the insulator-contact interfaces by either insulator energy band-gap grading, surface roughening, or through the use of multiphase materials such as Si-rich SiO_2. Experimental examples of each of these three cases will be discussed and novel applications in the area of electronic devices using these phenomena will be presented.

1. Introduction

Insulators such as SiO_2, Al_2O_3, or Si_3N_4 with large energy band gaps of approximately 9 eV [1], 9 eV [2], and 5 eV [3], respectively, have been used extensively in the electronics industry for passivation or as part of the active region of devices. With the advent of planar Si technology, SiO_2 which can be easily thermally grown from Si or deposited from a chemical vapor phase, has become the most important insulator, particularly in the gates of insulated-gate field-effect-transistors (IGFETs) which are used extensively for memory and logic operations. SiO_2 has also been shown to be superior to Al_2O_3 and Si_3N_4 in terms of its low trap densities in the forbidden gap for either electrons in the conduction band or holes in the valence band [4] and in terms of the number of interface states formed when contacted to semiconductors such as silicon [5]. Al_2O_3 and Si_3N_4 have been used particularly as charge storage layers in non-volatile memories where the carriers are tunneled into and out of these insulators by means of a thin ($\simeq$ 25 Å) tunnel oxide region grown on a Si substrate [6]. Also SiO_2 has a high mobility of 20-40 cm^2/V-sec as compared to other insulators for electrons once they are injected from the contacts into the SiO_2 bandgap [4]. Effective hole mobilities are much less in SiO_2 [4].

Large energy bandgap insulators form large energy barriers with contacting metals or semiconductors. This property causes the good insulating properties usually observed. Many solid-state devices require this blocking contact behavior. For instance, in an n-channel IGFET channel electrons flowing from the source to drain regions are kept confined to the Si surface layer by using SiO_2 between the channel and the gate electrode whose voltage is capacitively coupled to the Si by means of the SiO_2 layer.

There is, however, a class of devices where a dual nature (both insulating and conducting) of the insulator is required. These devices are used in non-volatile memories where information storage is needed for very long periods of time which requires the use of good insulators. The stored information usually takes the form of electrons or holes trapped on a metal-like layer buried in the SiO_2 gate insulator of an IGFET [7]. This metal-like layer usually is degeneratively doped n-type polycrystalline Si (poly-Si) [7]. The charge state of storage layer affects the operation of the transistor by its internal field and therefore performs a memory function. To write or erase the charge storage layer, carriers must be exchanged through the insulating layers with the metal or Si contacts. This is difficult because of the large energy barriers at the contacts of the materials used for the insulating layer, such as SiO_2. Injection into the insulator usually requires heating of the carriers in the metal or semiconductor using photons [4] or electric fields [4] so that the excited carriers can surmount

the energy barriers. Also if very large electric fields are applied, carriers can tunnel from near the top of the Fermi level for metals or from near the bottom of the conduction band (electrons) and the top of the valence band (holes) for semiconductors into the SiO_2 energy bands [4,8]. An alternative approach would be to devise an insulator system with a dual nature where the material is highly blocking to carrier injection from the contacts at low electric fields where the device would be normally read (that is, the charge state of the storage layer is sensed) and memory retention is required. However, the material must allow high current injection into the insulator from the contacts at higher electric fields when writing or erasing of the charge storage layer is required. This review will be concerned with such a class of insulating systems, the way to achieve this dual physical nature in practice, and experimental structures using these concepts.

II. High Current Injection

In this section, high current injection into insulators at low to moderate electric fields will be discussed for insulator-contact systems where the insulator energy band-gap is graded [9,10], the contact forms a rough surface with the insulator [11,12], or the insulating material at the interfaces with the metal or semiconductor contacts has at least two phases [13,14]. In the following section III, an experimental example of an electrically-alterable read-only-memory (EAROM) using the two phase system approach [15,16,17] will be presented in detail.

A. Graded Energy Band-gap

The idea of grading the energy band-gap of materials to obtain novel devices has been prevalent in the area of semiconductors [18]. Recently, this idea has been extended to insulators [9,10] as depicted schematically in Figs. 1 and 2 for a metal-insulator-semiconductor (MIS) system. Figure 1 shows the graded insulator system with no applied voltage dropped across the insulators. Figure 1a shows a homogeneous insulator, Fig. 1b shows a stepped insulator system with two insulators with different energy band-gaps, and Fig. 1c shows a graded insulator system which is just that of Fig. 1b in the limit of a large number of very thin stepped insulators from the bulk insulator to the metal contact. Figure 1 shows these systems with no applied voltage dropped across the insulators, while Fig. 2 depicts the band bending that occurs when a negative voltage is applied with respect to the metal contact. At low electric fields, as depicted in Fig. 1, a tunneling electron from near the top of the Fermi level of the metal electrode "sees" effectively the largest energy barrier of the insulating system (namely, that of the bulk insulator). However, when enough voltage is

applied to bring about the band bending shown in Fig. 2, a tunneling electron "sees" the lowered energy barrier at the metal contact with the graded energy band-gap system. In addition, the tunneling distance is smaller in the graded system (comparing Fig. 2a and 2c for the same bulk insulator electric fields. Clearly, a large tunneling current enhancement into the insulator conduction band from the metal contact is expected for the graded system as compared to a homogeneous insulator. This is demonstrated in Fig. 3 where calculated Fowler-Nordheim tunneling current density [19] as a function of the average electric field is shown for several insulating systems linearly graded from bulk SiO_2 to various energy band-gaps with respectively different contact-insulator energy barriers as indicated in this figure. Also, the calculations shown in this figure assume that the dielectric constant of the insulators increases linearly to the final value indicated with decreasing energy band-gap which is consistent with experimental observations for most materials of interest in the semiconductor industry.

Several experimental attempts have been made to obtain insulating systems graded from SiO_2 to Si_3N_4 [9,10]. DiMaria tried to do this using an As implant to smooth the SiO_2–Si_3N_4 interface energy step [9] (see Figs. 1b and 2b), while Hijiya et al. have reported that they obtained grading through oxynitride phases from Si_3N_4 to SiO_2 by oxidizing Si_3N_4 that had been grown by nitridizing Si with NH_3 at temperatures $\gtrsim$ 1000°C [10]. Both of these attempts at band-gap grading were incorporated into EAROM devices which worked similarly to what was expected if band-gap grading had occurred [9,10,19]; that is, either electron injection to charge, or hole injection to discharge (depending on applied gate voltage bias) a storage layer (discrete traps [9] or a floating poly-Si layer [10]) in the bulk of the SiO_2 via a graded energy band-gap insulator system near one of the contacting electrodes. However, no direct measure of the different interfacial energy barriers, using internal photoemission [13], has been reported.

B. Surface Roughness

Another way to get high current injection into an insulator at low to moderate average applied electric fields from a contacting electrode is by using surface roughness at the contact-insulator interface [11,12]. A rough semiconductor or metal surface with many hillocks or asperities will locally produce large electric fields near the tips of the asperities which decrease to the average applied field value in the bulk of the insulator. The local field enhancement must extend out at least a tunneling distance into the insulator; for example, 20-50 Å in SiO_2. The size, shape, and density of the asperities will affect the amount of local electric field enhancement which in turn controls the injected current density [20]. The integrated effect of

the local current injection over the entire contact area can easily produce many orders of magnitude increase in the average areal current density as compared to a similar structure with a planar interface. This is due to the strongly field-dependent tunneling current mechanism which is operative at all contact interfaces with wide energy band-gap insulators, at least initially.

The top surface of poly-Si films which are used extensively in the semiconductor electronics industry, are always naturally rough due to the many randomly oriented crystalline grains. If a thermal SiO_2 layer is grown on top of the poly-Si or a chemically-vapor-deposited (CVD) SiO_2 film is put down on this surface, high current injection from the asperities is always seen as shown in Fig. 4. The electric field enhancement for applied voltage biases favoring injection from the rough poly-Si surface is always larger than injection from the other insulator interface (see Fig. 4) which usually has some roughness (particularly on thin films) due to partial replication of the rough poly-Si surface by the insulator [11]. When deposited or grown on rough surfaces, insulators with many trapping states in their forbidden band-gap (such as CVD Si_3N_4) will usually screen the effect of the locally high electric fields by building up trapped space charge near the injecting tips of the asperities [21]. An experimental example of this phenomena is shown in Fig. 5 where a discrete tungsten trapping layer is sandwiched between a $\approx$ 70 Å thermal SiO_2 layer grown over a rough poly-Si surface and a 520 Å CVD SiO_2 capping layer [21]. This tungsten trapping layer readily captures electrons into energetically deep trapping sites with respect to the bottom of the SiO_2 conduction band, and screens the locally high fields of the asperities as shown in Fig. 5 where the areal current density is shifted to larger average electric fields (compare curves A and C). The CVD SiO_2 capping layer by itself also contains trapping sites due to H_2O incorporated into the film during deposition [4,14,21], and it will also screen the high local fields. These traps however have a lower electron capture probability and are further away from the asperities than the tungsten sites, and therefore will not be as effective as is seen in Fig. 5.

The surface roughness of the top surface of poly-Si layers used in Si-gated devices has been used to advantage in some devices (particularly EAROMs [22,23]) and reduced in others to minimize current leakage [12,24]. Many floating poly-Si gate memory type devices which are variations of the original floating-gate avalanche-injection metal-oxide-semiconductor (FAMOS) device introduced by Frohman-Bentchkowsky [7] use the rough poly-Si asperities to "erase" the floating poly-Si gate by removing the electrons, via the high local electric fields, to a top metallic or poly-Si control gate electrode [22,23]. One novel device used in a non-volatile memory operation has three levels of poly-Si (two rough top surfaces are used) where

both writing (putting electrons on) and erasing (taking electrons off) the floating poly-Si storage layer is achieved by electric field distortion caused by poly-Si surface roughness [25].

However, other types of devices using buried poly-Si gate electrodes which require low current leakage near the poly-Si surfaces have these surfaces fabricated as smooth as possible. A reduction in asperity size and probably aspect ratio (sharpness of the asperity) has been demonstrated by Anderson and Kerr [12] for oxides grown thermally at 1150°C above poly-Si surfaces. They also showed a reduction in the enhanced current injection consistent with the surface smoothing directly observed with scanning-electron-microscopy (SEM) [12].

C. Two Phase Materials

The final means to be discussed for achieving high current injection into an insulator at low to moderate applied fields involves incorporating a region inbetween the contact and insulator which is composed of a two phase material having semiconductor or metallic regions mixed into an insulator matrix. CVD Si-rich SiO_2 [26] or semi-insulating polycrystalline silicon (SIPOS) doped with oxygen atoms [27] which is a two phase mixture of Si and SiO_2 [28-31] that can be deposited from gaseous mixtures of N_2O and SiH_4 is one example. Cermets or granular metal films composed of insulating regions of such materials as SiO_2, Al_2O_3, or Si_3N_4 and metallic grains of such materials as Al, Ni, W, Au, Pt, Pd, or Mo which can be co-deposited by electron beam evaporation or sputtering systems [32] are other examples. With this type of insulator system, the cermet or Si-rich SiO_2 layer is fairly insulating at very low applied fields, but at larger electric fields it becomes very conductive compared to the underlying wide band-gap insulator and readily moves carriers from one metal or semiconductor island to another via Poole-Frenkel conduction, direct tunneling, or percolation until the interface of the cermet or Si-rich SiO_2 layer with the wide band-gap insulator is reached [13]. At this interface, electric field distortion will occur if the metal or semiconductor islands there have any curvature [13]. Figure 6 depicts this physical mechanism using energy band diagrams.

Recently, several publications from the IBM laboratory [13,14] have demonstrated this concept using a two phase mixture of Si and SiO_2 (Si-rich SiO_2). Examples of high electronic injection currents into a wide band-gap insulator of SiO_2 achieved with this system for various mixtures of Si-rich SiO_2 materials are shown in Fig. 7. The region in Fig. 7 from 0 V to −20 V for these structures is due to electron injection from the Al contact into the Si-rich SiO_2 layer and subsequent charging of the Si islands. The region beyond −20 V is due to

field-enhanced electronic Fowler-Nordheim tunneling off the last layer or layers of Si islands in the Si-rich SiO_2 material into the underlying thicker SiO_2 layer [13,14].

Further experiments by the IBM group demonstrated that stacked vertical layers composed of Si-rich SiO_2, SiO_2, and Si-rich SiO_2 could be formed using CVD techniques [15]. Enhanced electron injection from either the bottom contact (Si substrate) or the top contact (Al metal gate) for positive and negative gate voltage biases, respectively, could be obtained by means of the appropriate Si-rich-SiO_2–SiO_2 interfacial region in these structures [15]. The measured current-voltage characteristics for these dual electron injector structures, called DEISs, were also shown to be equivalent to the appropriate enhanced injection current-voltage characteristic observed on similar structures with just one Si-rich SiO_2 layer present [15].

These DEISs also exhibit an asymmetry in the enhanced electron injection from the Si-rich-SiO_2–SiO_2 interfaces (the bottom interface gives larger currents than the top interface for the same average electric fields) even though the CVD Si-rich SiO_2 regions of the DEIS stack were fabricated under identical conditions [15]. This asymmetry is believed to be due to the fact that the bottom Si-rich SiO_2 layer is deposited on Si which is either crystalline or polycrystalline, while the top layer is deposited on top of SiO_2 which is amorphous [15]. Cross-section transmission-electron-micrographs (CRTEM) have shown evidence for a "rougher" interface with the SiO_2 layer for the bottom Si-rich SiO_2 layer which also appears to have larger and denser numbers of Si islands than the top Si-rich SiO_2 layer [17,33,34].

In the very low field region, the cermets or Si-rich SiO_2 layers cause another interesting effect. The very small metal or semiconducting islands in these layers act as charge trapping sites for carriers injected at very low fields due to asperities or particulate on the contact; and they field screen these weak spots by the space charge they build-up [17,21,33] (see section II-B). This space charge is not permanent, but it can move back to the contact when the electric fields are reversed [13,17]. Capacitor structures using Si-rich SiO_2 layers inbetween the contact and bulk SiO_2 have been shown to give outstanding breakdown histograms due to this phenomenon with very few low field breakdown events as compared to control structures processed identically but without the Si-rich SiO_2 layers present [13,33].

In the next section, experimental examples of EAROM structures using DEIS stacks between floating and control gate poly-Si layers will be discussed in detail.

III. DEIS EAROMs

The DEIS EAROM is a non-volatile semiconductor memory which uses the high current injection from the Si-rich-SiO_2–SiO_2 interfaces of a DEIS stack to charge or discharge a floating degenerate n-type poly-Si storage layer as depicted in Fig. 8 [15-17,33]. Negative control gate voltage biases are used to charge (write operation) the floating poly-Si by injecting electrons onto it while positive control gate voltage biases (erase operation) are used to discharge it by pulling electrons off of it. Over erasure is also possible by leaving the poly-Si in a state with a net positive charge due to ionized donors.

The cycling (write/erase) characteristic of such a DEIS EAROM is shown in Fig. 9 where positive threshold voltages of the device indicate stored electrons on the floating poly-Si while negative threshold voltages indicate ionized donors [35]. Clearly from this figure the device can be written and erased approximately 10^4 times before the threshold voltage starts to degrade and collapse. This collapse is caused by electron capture on energetically deep trapping sites in the band-gap of the intervening CVD SiO_2 layer [4,14,15,33]. These traps are believed to be related to H_2O impurities incorporated into the CVD SiO_2 layer during fabrication [4,36,37] and their number can be reduced by high temperature (1000°C) annealing in nitrogen or forming gas (N_2/H_2 mixtures) prior to the control gate deposition [15,17,37]. The cycling characteristic can be recovered by thermally discharging the electrons trapped on these sites by using mild heating in forming gas or room air with temperatures between 200°C and 400°C [33]. Also, recovery can be obtained by applying larger gate voltages to return the electric fields nears the Si-rich-SiO_2–SiO_2 interfaces (which have been lowered by the internal fields of the trapped charge) to the values they had initially [33] as shown in Fig. 9.

Because of the very low voltages at which the device gate is held when not in use, the retention characteristics (perturbation of the stored information by charge leakage off of the floating gate) of the DEIS EAROM is excellent [16,33] because of the insulating behavior of the Si-rich SiO_2 regions in this voltage regime (see section II-C). Also, since the voltages at which the device is read (that is, the stored information on the floating poly-Si layer is sensed by the conduction of the Si surface channel between the source and drain of the transistor) are low ($\leq$ 5 V), read perturb effects due to electron removal off the floating poly-Si by tunneling are negligible [33].

The DEIS EAROMs also have excellent breakdown characteristics, particularly in minimizing low voltage breakdown events [16,17,33], due to the field screening action of the Si-rich SiO_2 layers as was discussed in section II-C. This ability of the DEIS stacks to pass very high electronic particle densities allows them to be written or erased in very short times

as shown in Fig. 10. This figure demonstrates 20 ns operation which is the fastest time ever reported for switching an EAROM electronically in a non-destructive manner.

Other types of DEIS EAROMs can be fabricated with the DEIS stack over the channel region of the device rather than between the control and floating gate electrodes. However, this structure has the disadvantage that the Si islands in the Si-rich SiO_2 layer will act similarly to "slow" surface states by capturing carriers from the channel region and building up an electric field which will degrade device performance. If the device is read in times that are short compared to those necessary for most of the nearest Si islands to capture electrons, then the device performance will not be as severely degraded as shown in Fig. 11.

Another interesting phenomenon associated with the reversible trapped space charge which builds up on the Si islands in the Si-rich SiO_2 layers of DEIS stacks is the injection efficiency degradation shown in Fig. 12. The effect demonstrated in this figure is due to trapped electrons building up in the Si-rich SiO_2 region near the injecting contact, screening the electric field, and thereby lowering the injection efficiency from the contact. This phenomenon is more pronounced if the Si-rich SiO_2 layer is thick and/or has a small percentage of excess Si so that these trapped electrons can not move as easily through the Si-rich SiO_2 layer to the Si-rich-SiO_2–SiO_2 interface and then be injected into the SiO_2 layer (compare Figs. 12 and 13). Clearly in Fig. 12, a longer delay between each pulse of a string of write or erase pulses gives a larger threshold voltage shift magnitude since more electrons are put onto or removed from the floating poly-Si layer. This is because the trapped electrons on the Si islands which block contact injection have had sufficient time to move back to the appropriate contact possibly having this motion influenced by their own internal electric field. Figure 12 also shows that a large number of pulses of small duration are more efficient than one large pulse of the same total time duration. Again this is due to the trapped electronic charge build-up on the Si islands limiting contact injection particularly when there are few, small duration, or no delays between each pulse of the write or erase pulse train. Another phenomenon closely related to that depicted in Figs. 12 and 13 occurs during sequential write/erase cycling with single pulses of DEIS EAROMs [33]. In this case, if the delay time from write to erase pulse (or vice versa) is too short, the electric field generated by the trapped electronic space charge in the opposite Si-rich SiO_2 injector which was used during the previous write or erase operation decreases the electric field near the Si-rich-SiO_2–SiO_2 interface which is being used currently [33]. This phenomenon is more pronounced on DEIS EAROMs with thin SiO_2 regions and thick and/or low excess Si content Si-rich SiO_2 regions [33].

IV. Conclusions

This review has been concerned with a means of obtaining high current injection into wide band-gap insulators such as SiO_2, Si_3N_4, or Al_2O_3 at low to moderate electric fields using a modification of the contact-insulator interface. This modification has been obtained by generating locally high electric fields or by grading the insulator energy band-gap. Other materials and means for doing this will probably evolve in the future because of the need for such insulating systems in the area of non-volatile semiconductor memory. Electrically alterable memories such as the one described in section III will find increasing use in electronic equipment requiring microprocessors which should rapidly develop in the 1980's. The EAROMs described here may evolve into pure non-volatile random-access-memories (NVRAMs) if the cycling degradation problem due to charge trapping in the SiO_2 layer can be solved and large numbers of cycles ($\gtrsim 10^{12}$) are obtained.

ACKNOWLEDGEMENTS

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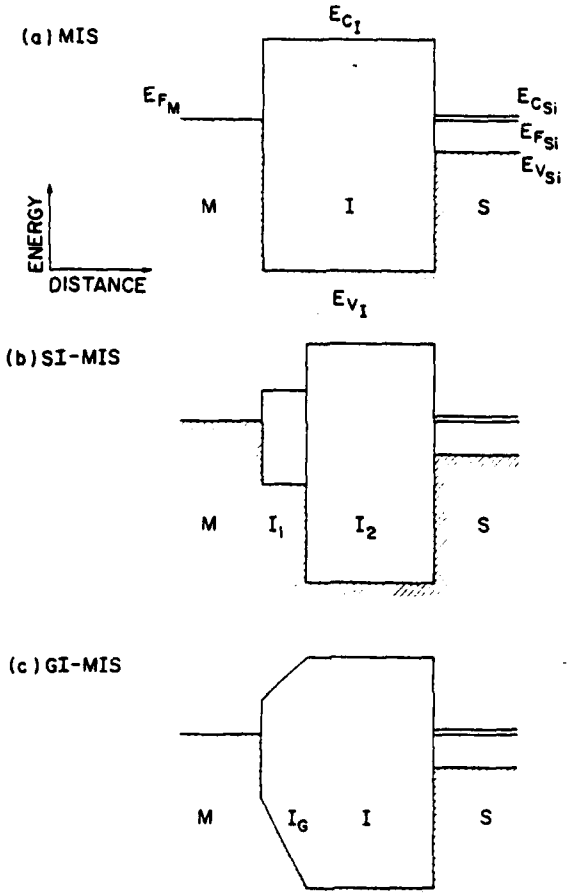

Fig. 1: Zero applied field energy band diagram for (a)-MIS, (b)-stepped insulator (SI-MIS), and (c)-graded insulator (GI-MIS) structures. Taken from Reference 9.

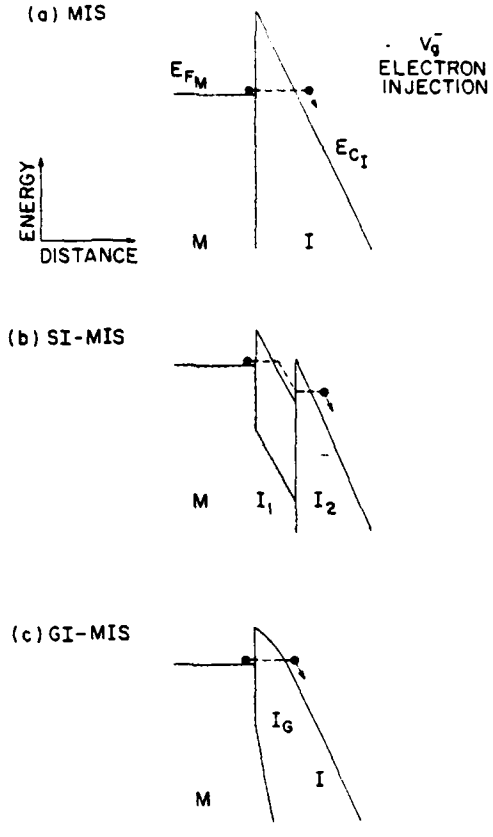

Fig. 2: Energy band diagram for negative gate bias (electron injection from the gate electrode) for (a)-MIS, (b)-stepped insulator (SI-MIS), and (c)-graded insulator (GI-MIS) structures. Taken from Reference 9.

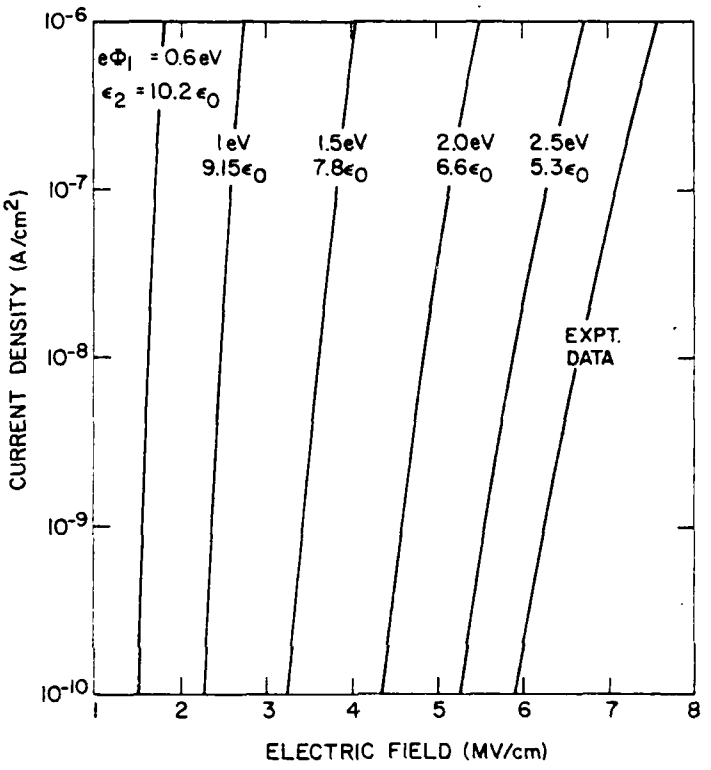

Fig. 3: Magnitude of the areal particle current density injected into the conduction band of a graded band-gap insulating system as a function of the magnitude of the average applied electric field. The energy barrier at the contact-insulator interface is graded linearly from the value assumed for SiO_2, which is 3.1 eV, to the values indicated on the various curves by $e\Phi_1$. Also the low frequency dielectric constant is increased linearly from that of SiO_2 which is 3.9 to the values assumed at the contact-insulator interface which are also indicated on the curves by the numerical factor in the expression for ϵ_2 with ϵ_0 being the permittivity of free space. The grading is assumed to be done over 500 Å of insulating material.

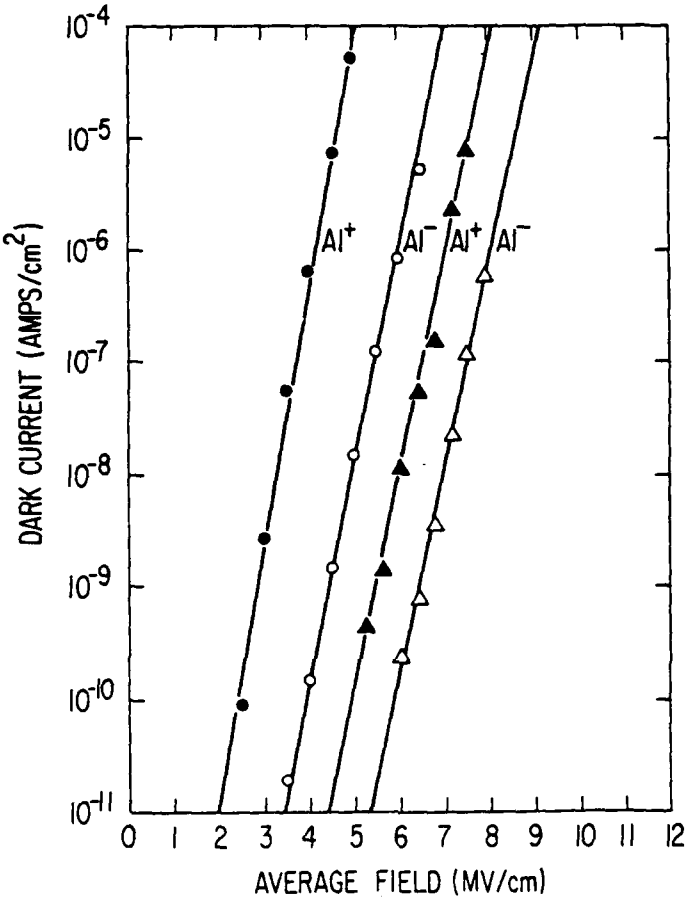

Fig. 4: Point by point magnitude of the areal dark current density as a function of the magnitude of the average electric field in the oxide for polycrystalline and single crystal Si-SiO_2-Al MOS structures with 500 Å oxide layers grown at 1000°C in O_2. The data were generated by measuring the current in the external circuit 2 min. after each .5 MV/cm step increase in the magnitude of the average electric field starting at 0 V.

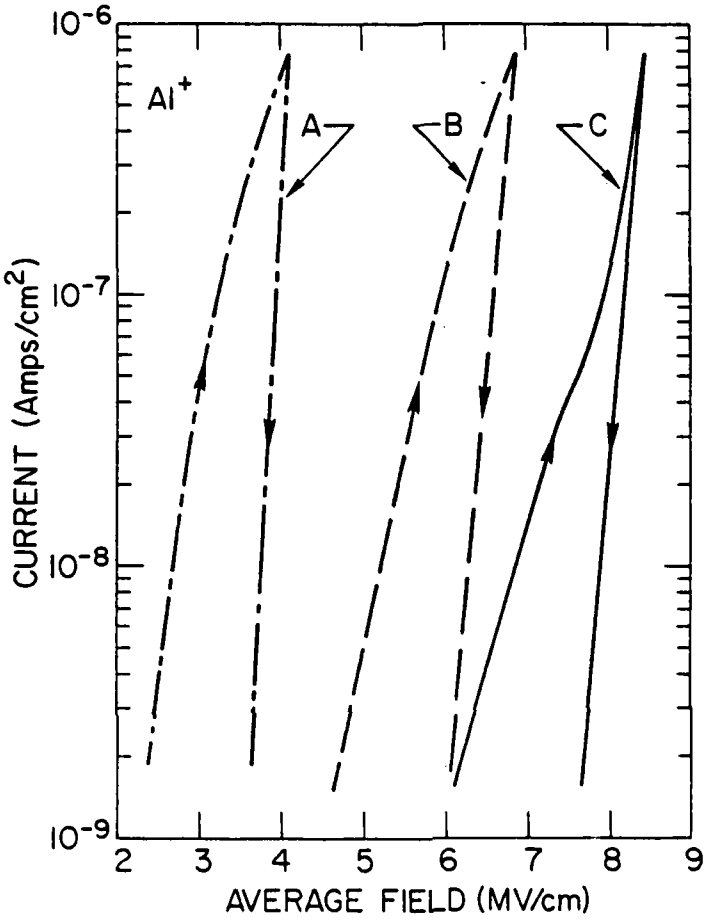

Fig. 5: Ramped magnitude of the areal dark current density measured in the external circuit as a function of the magnitude of the average electric field for positive gate bias and a ramp rate of 9.5 x 10^{-3} MV/cm-sec. Composition of MOS samples A, B, and C are:

A: Al - thermal SiO_2 (450 Å) - poly Si

B: Al - CVD SiO_2 (520 Å) - thermal SiO_2 (70 Å) - poly Si

C: Al - CVD SiO_2 (520 Å) - W ($\simeq 10^{14}$ atoms/cm^2) - thermal SiO_2 (70 Å) - poly Si.

Taken from Reference 21.

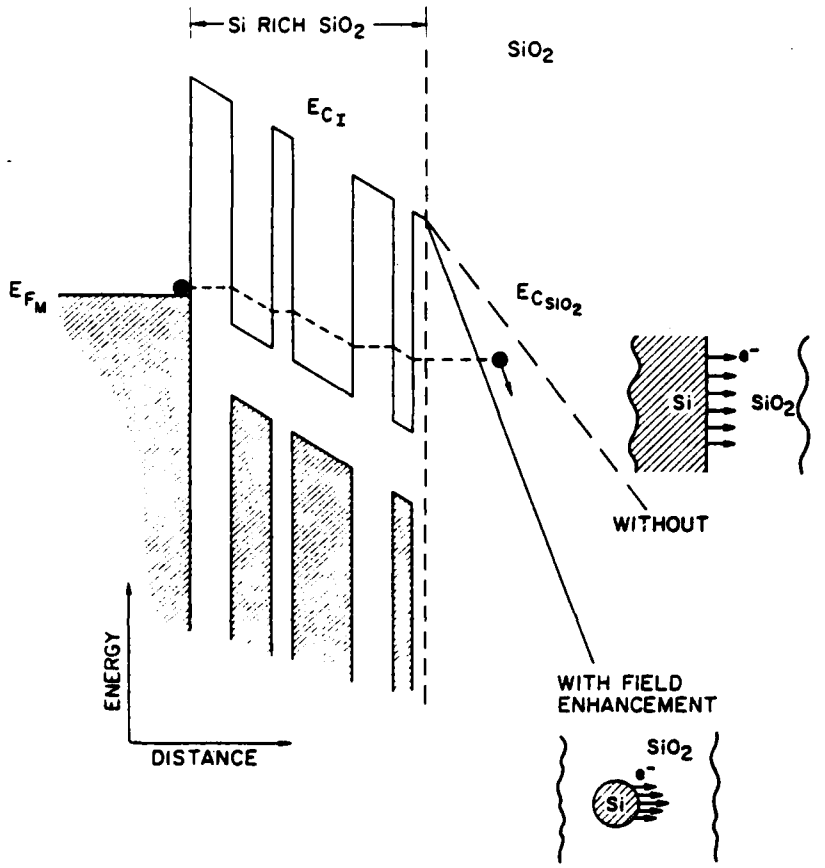

Fig. 6: Schematic energy band representation of conduction in the Si-rich SiO_2 layer via direct tunneling between isolated Si regions in the SiO_2 matrix of this two phase system and subsequent high field injection into the underlying SiO_2 region due to local electric field enhancement caused by the curved surfaces of the Si regions. Electronic Fowler-Nordheim tunneling into SiO_2 from a planar Si surface is shown for comparison. Taken from Reference 17.

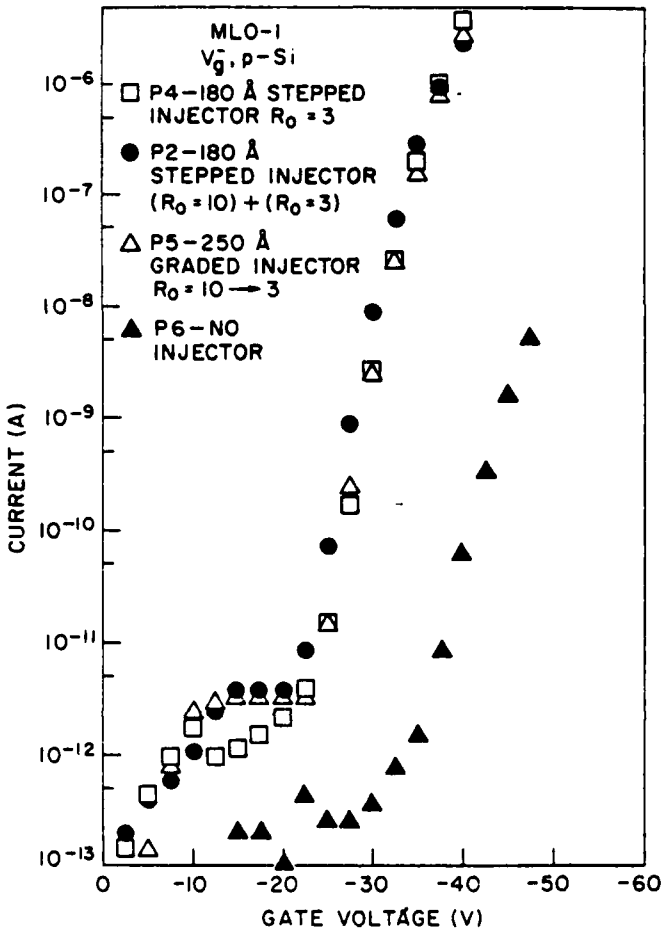

Fig. 7: Point by point magnitude of the dark current as a function of negative gate voltage on various GI-MIS and SI-MIS structures. In this measurement, the gate voltage was stepped by −2.5 V starting from 0 V every 20 sec with the dark current being measured 18 sec after each voltage step increase. The Si-rich SiO_2 layer was either stepped or graded with R_o defined as $[N_2O]/[SiH_4]$ as an indicator of the Si content of this layer. R_o from 10 (40% atomic Si) to 3 (46% atomic Si) was used with Si content increasing towards the top metal gate electrode when several layers were stacked on top of the underlying 550 Å thick thermal SiO_2 layer ($R_o = 10 + 3$) or when a graded layer was used ($R_o = 10 \rightarrow 3$). Taken from Reference 13.

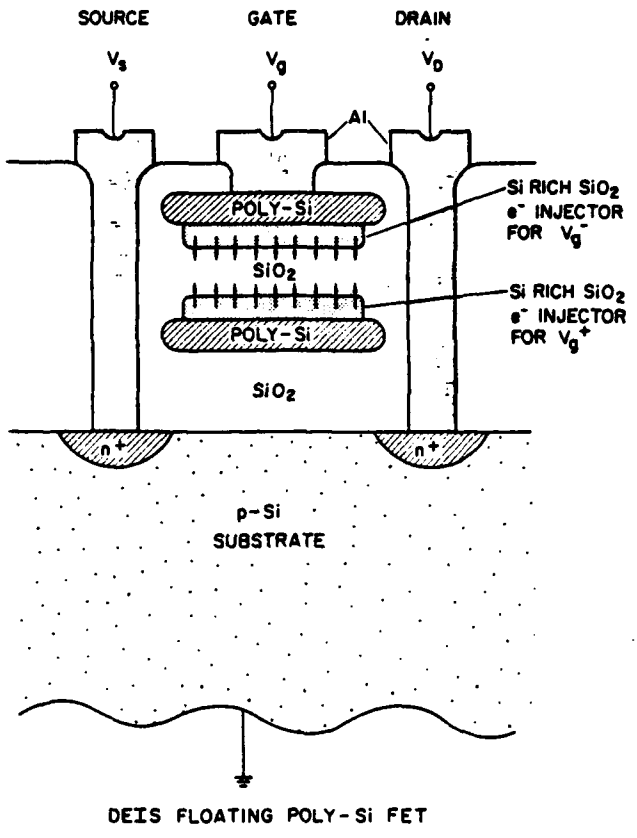

Fig. 8: Schematic representation of a non-volatile n-channel field effect transistor memory using a dual electron injector stack between a control gate and a floating poly-Si layer. Writing (erasing) is performed by applying a negative (positive) voltage, V_g^- (V_g^+), to the control gate which injects electrons from the top (bottom) Si-rich SiO_2 injector to the floating poly-Si storage layer (back to the control gate). Structure is not drawn to scale. Taken from Reference 15.

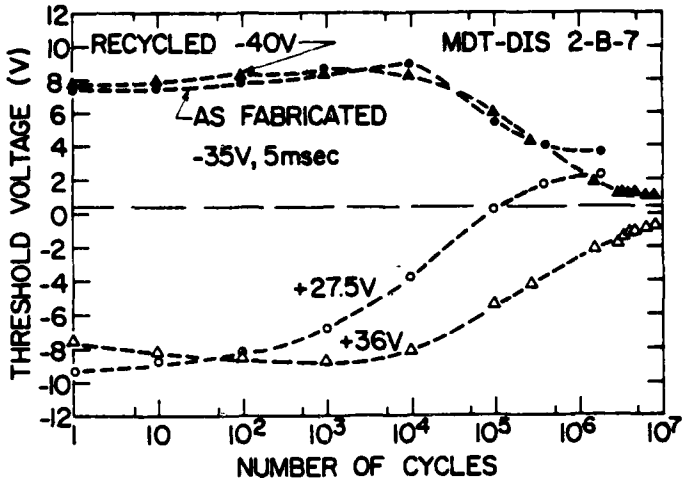

Fig. 9: Threshold voltage after writing and erasing as a function of the number of write/erase cycles on an n-channel DEIS FET from wafer MDT-DIS 2-B (290 Å gate oxide from the floating poly-Si layer to the Si substrate and a CVD DEIS stack of 150 Å Si-rich-SiO_2–150 Å SiO_2–150 Å Si-rich-SiO_2 from the floating poly-Si to control gate poly-Si with the Si-rich SiO_2 having 46% atomic Si). Solid and open symbols correspond to the threshold voltage after writing at −35 V and erasing at +27.5 V for 5 msec, respectively, the as-fabricated structure. Solid and open triangles correspond to the threshold voltage after writing at −40 V and erasing at +35 V for 5 msec, respectively, the same structure after threshold window collapse due to charge trapping in the intervening CVD SiO_2 layer of the DEIS stack. The horizontal dashed line indicates the initial threshold voltage of the as-fabricated FET before cycling.

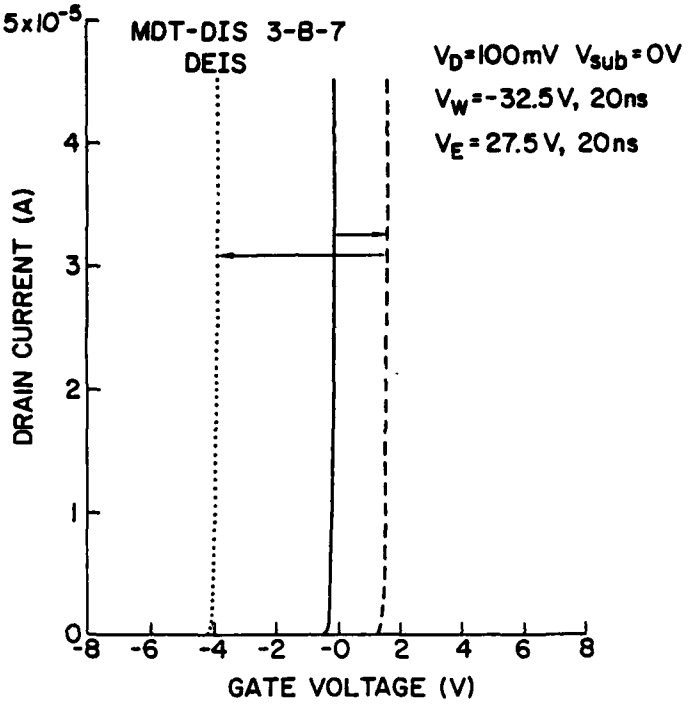

Fig. 10: Drain current as a function of the gate voltage with the drain biased at V_D = 100 mV and the source and substrate grounded $V_S = V_{sub} = 0$ V on an n-channel DEIS FET from wafer MDT-DIS 3-B (100 Å gate oxide from the floating poly-Si layer to the Si substrate and a CVD DEIS stack of 100 Å Si-rich-SiO_2–100 Å SiO_2–100 Å Si-rich-SiO_2 from the floating poly-Si to the control gate poly-Si with the Si-rich SiO_2 having 46% atomic SiO_2). The device was first written with −32.5 V in 20 ns from its virgin uncharged state and then erased with +27.5 V in 20 ns as indicated by the arrows.

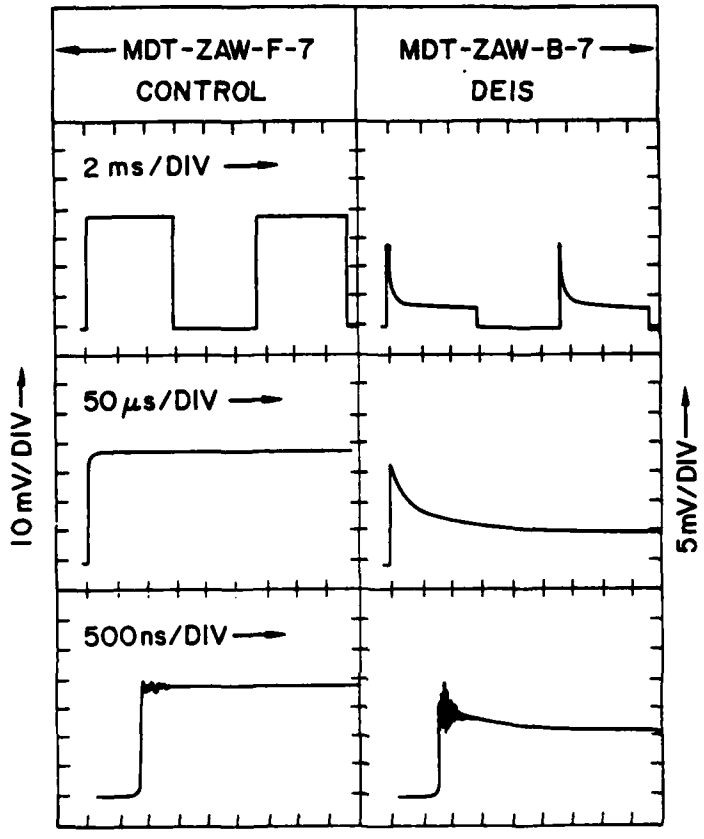

Fig. 11: Oscilloscope traces of the drain current flowing due to a 5 V step applied to the control gate as a function of time with V_D = 100 mV and V_S = V_{sub} = 0 V on n-channel DEISs and control FETs from wafers MDT-ZAW-B,F. Wafer B has the CVD DEIS stack (100 Å Si-rich-SiO_2–500 Å SiO_2–100 Å Si-rich-SiO_2) as the gate insulator between the Si substrate and the control gate poly-Si electrode, while the control wafer has just the CVD 500 Å thick layer of SiO_2 as the gate insulator. These traces show that the FET operation is not too severely deteriorated due to the Si islands in the Si-rich SiO_2 layer deposited on the substrate Si acting as surface states if the operating time is kept in the hundreds of nanoseconds regime.

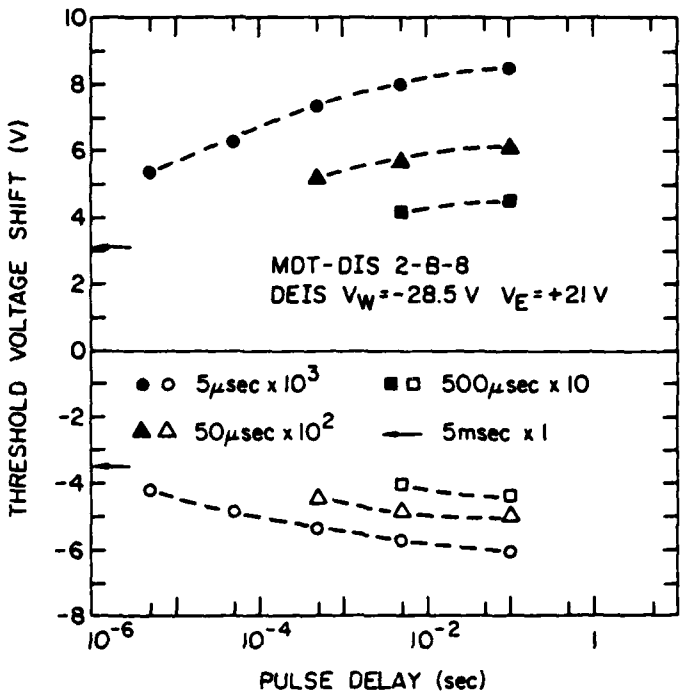

Fig. 12: Threshold voltage shift as a function of the time delay between write or erase pulses for pulse trains of various time durations but all adding to 5 msec on an *n*-channel DEIS FET from wafer MDT-DIS 2-B which was described in the caption of Fig. 9. Each point was taken by either writing with a voltage of −28.5 V (as indicated by solid symbols) or erasing with a voltage of +21 V (as indicated by open symbols) using the number of pulses with the indicated pulse time duration listed opposite the appropriate symbols. Prior to each write or erase measurement, the device was reset into an opposite charge state (for example, an ionized donor state on the floating poly-Si prior to a write pulse train). The device was reset to the same opposite charge state for each write or erase measurement by cycling about 25 times with −28.5 V and +21 V and then stopping after the appropriate write or erase pulse.

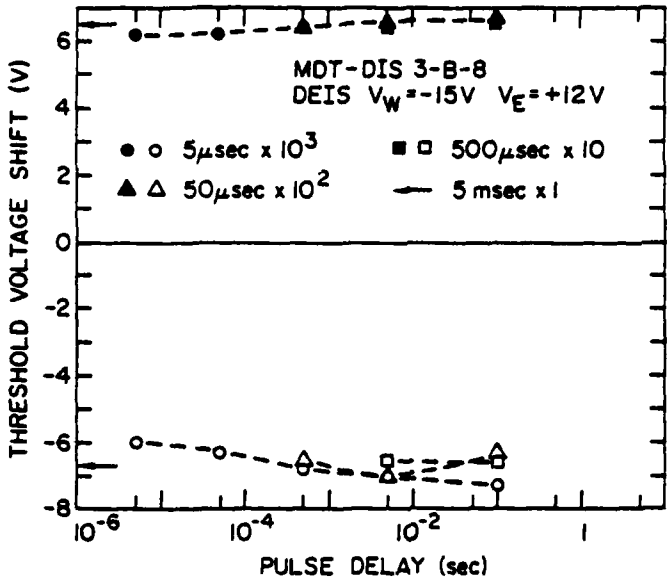

Fig. 13: Threshold voltage shift as a function of the time delay between write or erase pulses for pulse trains of various time durations but all adding to 5 msec on an n-channel DEIS FET from wafer MDT-DIS-3B which is described in the caption of Fig. 10. Symbols have the same meanings as in Fig. 12, but with write or erase voltages of −15 V or +12 V, respectively.

Electrically-Alterable Read-Only-Memory Using Si-Rich SiO_2 Injectors and a Floating Polycrystalline Silicon Storage Layer

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ABSTRACT

Currently, electrically-alterable read-only memory (EAROM) has become increasingly important for memory and logic operations. A novel EAROM device in a field effect transistor (FET) configuration which uses a floating polycrystalline silicon (poly-Si) storage layer on top of thermal SiO_2 and a dual electron injector structure (DEIS) between this floating poly-Si and a control gate poly-Si contact is described. The DEIS stack consists of sequentially chemically vapor deposited (CVD) layers of Si-rich SiO_2 (46% atomic Si), SiO_2, and Si-rich SiO_2 (46% atomic Si) between the poly-Si layers. Electrons from either poly-Si layer can move to the other poly-Si layer biased at the higher voltage with moderate applied voltages. Thus, the floating poly-Si storage layer can be charged with electrons ("write" operation) or with positive charge ("erase" operation) in msecs with negative and positive control gate voltages, respectively. The average electric fields in the intervening CVD SiO_2 layer during writing and erasing are 5-6 MV/cm and 4-5 MV/cm, respectively, and voltages from ± 10 V to ± 40 V can be used depending on the device configuration. The enhanced electron injection in these devices is believed to be controlled by localized electric field distortion at the Si-rich-SiO_2–SiO_2 interface caused by the two phase (Si and SiO_2) nature of the Si-rich SiO_2. The electrical asymmetry of the DEIS is believed to be due to differences in the interfaces of the bottom and top Si-rich SiO_2 injectors with the intervening SiO_2 layer. At the low voltages used for the "read" operation in which the charge state of the floating poly-Si layer is sensed by the FET drain current, no read perturb effects are observed. These structures also show excellent charge retention at low voltages, characteristic of a floating poly-Si storage layer surrounded by SiO_2. This excellent retention is due to a characteristic of the Si-rich SiO_2 in which it builds up a reversible space charge layer which collapses the field at the interface with the poly-Si layers and minimizes charge loss or further injection. This field screening phenomenon of the Si-rich SiO_2 layers also prevents low voltage breakdowns (which are believed to be due to irregularities in the field at the cathode) from occurring. These DEIS EAROMs operate at lower power due to the small injected SiO_2 currents involved and low applied voltages compared to most commercially available devices which use Si

junction avalanche injection which requires large Si currents to charge the floating poly-Si storage layer. These devices are capable of being cycled at least 10^4 times before pronounced threshold-voltage window collapse due to trapped electron space charge build-up in the intervening CVD SiO_2 layer.

I. Introduction

Non-volatile memory devices which can store information without an external power supply for long periods of time are currently an area of much interest [1-5]. Current trends show a large effort by the electronics industry to develop electrically-alterable memories where stored information can be changed "electrically" [1-5]. These memories are usually composed of a metal-oxide-semiconductor field-effect-transistor (MOSFET) configuration with a charge storage layer in the gate oxide region which can be charged-up with injected electrons (called the "write" operation). The channel current of the MOSFET which is sensitive to the internal electric field generated by these trapped electrons is used to determine whether the captured charges are present or not (called the "read" operation). To change the stored information, the electrons can be removed from the storage region in the gate oxide (called the "erase" operation) and new information can be written in. Electrically-alterable read-only-memories (EAROMs) have two specific requirements which tend to oppose each other. These requirements are to get charge into and out of a charge storage layer at low voltages and powers in times on the order of milliseconds (msec), but to have the capability of holding this stored charge as information for periods of time as long as years. This article will be concerned with describing such a class of devices using a new technology which satisfies both of these requirements. This new technology uses a thin interfacial layer of Si-rich SiO_2 [6-10] between an SiO_2 layer and an electrode to allow electrons to more easily tunnel into the SiO_2 layer through the large energy barrier normally present between the oxide and the electrode [11-13]. This allows devices to be written and erased at moderate voltages and low powers. At the lower voltages used to "read" devices, the stored charge remains unperturbed because further injection from one of these modified contacts is blocked by a reversible trapped space charge build-up in the intervening layer of Si-rich SiO_2 [12,13]. Before these structures are described in detail, other non-volatile devices will be discussed and compared.

Some of the newest memories use SiO_2 conduction to charge up the storage layer [usually a floating polycrystalline silicon (poly-Si) layer] which is surrounded by SiO_2 [2,3,14]. These structures use low power during writing and erasing because the oxide currents are small. They can be operated from 5 volt and 20 volt supplies [14] or from just a 5 volt supply by charge pumping up to the desired write and erase voltages [4]. One of the devices uses localized current injection into SiO_2 from asperities on the top surface of deposited poly-Si films to write and erase a floating poly-Si layer [15-17]. It is a large cell requiring 3 layers of poly-Si, and it can be written and erased with 30 V pulses in 2-4 msec between 10^3 to 10^5 times [2-4]. The other device, called the FLOTOX which is an abbreviation for floating gate tunnel oxide, uses Fowler-Nordheim tunneling of electrons from a planar Si-SiO_2 interface at

high electric fields (≈ 10 MV/cm). The voltage requirements for writing or erasing the FLOTOX in 10 msec have been reduced to 20 V by using very thin (≈ 200 Å thick) intervening SiO_2 layers from the floating poly-Si layer to the silicon crystal Si substrate with the thin oxide placed over a drain extension [14]. The FLOTOX device can be cycled 10^4-10^6 times [14]. The threshold voltage window collapse in both types of non-volatile memories is probably due to electron trapping in the intervening SiO_2 layers [18,19]. Both types of devices are restrictive in their fabrication requirements as opposed to the devices discussed here where the insulator stack used for writing or erasing can be placed anywhere in the device configuration. Reproducibility of the rough poly-Si surfaces and therefore the write and erase operations of the devices which use this material characteristic may also be a problem.

Most of the other commercially available devices using a continuous floating poly-Si layer use hot electron injection from a Si junction which is biased to an avalanche condition [5]. These structures are variations of the original floating-gate avalanche-injection MOS (FAMOS) introduced by Frohman-Bentchkowsky [20,21]. They require higher power because the Si currents are very large compared to the relatively low number of hot electrons which locally surmount the Si-SiO_2 interfacial energy barrier and get into the oxide conduction band. These locally injected electrons then drift in the applied electric field, are captured on the floating poly-Si layer, and then spread out uniformly over the poly-Si. Erasing these structures is usually difficult requiring high voltages and long times. Ultra-violet light [20-24], high electric fields at asperities on the top surface of the floating poly-Si [15,25], hole avalanche injection from a substrate Si junction [26], and recently even electron avalanche ejection from a p-type floating poly-Si layer [27] are used for erasure. These devices are typically written with about 20-35 V in ≳ 10 msec [5], although one structure using high temperature thermal nitridation of the Si substrate instead of thermal SiO_2 between the Si substrate and floating poly-Si layer has been reported to operate at ≈ 10 V in 1 msec due to lower interfacial energy barriers [28]. The localized nature of the avalanche current injection is sensitive to processing conditions. Surface states and positive charges are also observed to build-up near the injection point for either electrons or holes at the substrate Si-SiO_2 interface which is also usually the interface used to sense the stored charge on the floating poly-Si layer. Write or erase areas can be separated from the active channel of the MOSFET, but this results in larger cells and less dense arrays.

Some commercially available EAROM structures are based on the metal-thick silicon nitride-thin tunnel silicon dioxide-silicon (MNOS) structure [24]. These devices are written (erased) in a uniform fashion over the entire device area by tunneling electrons (holes) from

the Si substrate through the thin tunnel-SiO_2 layer into the Si_3N_4 where the carriers are trapped. Some of these structures can operate at speeds of less than 1 msec at gate voltages between 20-30 V and can be cycled (written and erased) about 10^5 times. However, MNOS structures are not as stable as a floating poly-Si storage layer surrounded by SiO_2 because charge stored in the Si_3N_4 layer will rearrange itself and leak-off in time due to the conductivity and bulk trapping properties of the Si_3N_4 [29]. Trapped carriers can also back-tunnel from near the Si_3N_4-SiO_2 interface to the Si substrate through the thin ($\simeq$ 25-30 Å) SiO_2 layer [30]. In addition, the thin tunnel SiO_2 layer must be uniformly, reproducibly, and accurately grown so that the device operating voltages remain within certain limits on a given wafer or from wafer to wafer.

II. Stepped or Graded Insulator Structures

Several recent publications by two of the authors (DiMaria and Dong) have demonstrated that Si-rich SiO_2 deposited on SiO_2 can give high current injection into the oxide conduction band at moderate applied gate voltages [11-13]. This phenomenon is believed to be caused by electric field distortion at the SiO_2–Si-rich-SiO_2 interface [12] due to the two phase (Si and SiO_2) nature of the Si-rich SiO_2 material [31-35]. Fig. 1 schematically depicts what is thought to occur. The Si-rich SiO_2 layer due to its lower resistivity compared to SiO_2 fills up with space charge at low voltages [12,13]. At higher, moderate voltages localized injection into the SiO_2 layer via Fowler-Nordheim tunneling from the closest Si islands in the Si-rich SiO_2 matrix can occur [12,13]. Since the Si islands have curvature, the electric fields near their surfaces are enhanced locally [12,13,16,36] and current injection is observed at much lower voltages than expected for a planar Si-SiO_2 interface. Since the Si regions are very small ($\lesssim$ 50 Å) [10,32] and densely packed for the 46% atomic Si material used in this study, the current injection "appears" uniform to a charge storage layer in the bulk of the SiO_2 layer [13]. A previous publication [12] has shown that at least for large area circular capacitor structures (6×10^{-3} cm^2) a "W" trapping layer sandwiched between SiO_2 layers could be charged with electrons with negative gate voltages using a Si-rich SiO_2 injector under the Al gate electrode. It was also observed that the stored electrons could not be annihilated easily (erase operation) using positive gate voltages because the hole energy barriers at a Si-SiO_2 interface, even with field enhancement, are very large ($\approx$ 5 eV compared to $\approx$ 3 eV for electrons [18]). In this study, small area (8.4×10^{-6} cm^2) enclosed MOSFET structures using a floating poly-Si storage layer which can be charged or discharged using a dual Si-rich SiO_2 electron injector structure [37] (referred to as a DEIS) in the region between the floating poly-Si and a control poly-Si gate electrode as is shown schematically in Fig. 2 will be

discussed. In this structure, erasure is accomplished under positive gate voltage bias by the Si-rich SiO_2 injector deposited on top of the floating poly-Si surface. Without this bottom erase injector present, erasure of electrons can still be accomplished at higher positive gate voltages by localized injection from the rough floating poly-Si top surface which has been known for several years [15-17, 25]. This device is referred to as a single electron injector structure (SEIS). Both types of Si-rich SiO_2 injector structures will be discussed in detail in sections IV-A and IV-B.

III. Experimental

A) Device Fabrication

The enclosed FET structures were fabricated using a self-aligned, double poly-Si process which will be described below. All of the devices used in this study, except where stated differently, had a channel length of 2.54×10^{-4} cm after photolithography, but effectively $\approx 1.8 \times 10^{-4}$ cm after diffusion drive-in and subsequent high temperature processing. The channel width was 1.62×10^{-2} cm and the FET channel area was effectively 2.9×10^{-6} cm^2. The actual injecting area for writing and erasing was 8.4×10^{-6} cm^2 due to capacitive considerations. After defining thick field oxide regions, the devices were fabricated by thermally oxidizing a 0.5 Ωcm <100> p-type single crystal silicon substrate to an SiO_2 thickness of either 435 Å, 290 Å, or 100 Å for the different device runs which are called MDT-113, MDT-DIS 2, and MDT-DIS 3, respectively. Next a 3,500 Å thick poly-Si layer was deposited and doped n-degenerate with $POCl_3$ (this will form the floating charge storage layer) followed by the injector stack consisting of CVD deposited SiO_2 and Si-rich SiO_2 layers as listed below from bottom to top for the various device runs:

MDT-113-A,A′	210 Å SiO_2
MDT-113-C,C′	210 Å SiO_2 – 90 Å Si-rich-SiO_2
MDT-DIS 2-A,B	150 Å Si-rich-SiO_2 – 150 Å SiO_2 – 150 Å Si-rich-SiO_2
MDT-DIS 2-C,D	150 Å SiO_2 – 150 Å Si-rich-SiO_2
MDT-DIS 2-E,F	150 Å SiO_2
MDT-DIS 3-A,B	100 Å Si-rich-SiO_2 – 100 Å SiO_2 – 100 Å Si-rich-SiO_2
MDT-DIS 3-C,D	100 Å SiO_2 – 100 Å Si-rich-SiO_2

MDT-DIS 3-E,F 100 Å SiO_2

A top 3500 Å thick poly-Si n-degenerate layer, similar to the first poly-Si layer, was then deposited and doped. Next, the gate stack was etched with plasma etching, reactive ion etching (RIE), and wet etching to define the source and drain. The source and drain were diffused, a 1000 Å oxide was regrown at 1000°C over the source and drain, and a protective 3000 Å layer of CVD SiO_2 followed by a phosphosilicate glass (PSG) passivation layer were deposited and annealed at 1000°C. Finally, contact holes to the source, drain and top poly-Si gate were defined and etched, followed by Pd_2Si and Al metallizations and a 400°C anneal for 20 minutes in forming gas (90% N_2 - 10% H_2). All CVD Si-rich SiO_2 layers contained 46% atomic Si and were deposited at 700°C using a ratio of concentrations of N_2O to SiH_4 in the gas phase, R_o, of 3 [12,31]. All CVD SiO_2 layers were deposited at 700°C using a concentration ratio of N_2O to SiH_4 in the gas phase of 100. Annealing prior to metallization at 1000°C for the capacitors or subsequent processing of the FETs involving 1000°C thermal cycles after control gate poly-Si deposition converts many of the amorphous Si regions in the Si-rich SiO_2 layers to Si crystallites [38,39] and removes many of the H_2O related trapping sites from the CVD SiO_2 layers [13,18,19,37,40]. This annealing does not effect the injection efficiency of the Si-rich SiO_2 injectors [12], but it does increase the cyclibility of the devices by reducing charge trapping in the intervening CVD SiO_2 layer as will be discussed here.

Some large area capacitor structures were also fabricated for comparison, breakdown, and reproducibility studies. CVD 200 Å Si-rich-SiO_2 – 400 Å SiO_2 – 200 Å Si-rich-SiO_2 DEIS layers were deposited on .5 Ωcm <100> p-type single crystal Si substrates. The structures were then annealed in N_2 at 1000°C for 30 min prior to circular, .006 cm^2 area, Al gate metallization. Finally, a 400°C forming gas anneal for 20 min was performed. Control structures with only a CVD 400 Å thick SiO_2 layer which otherwise received identical processing were also fabricated. Other sets of capacitors for similar experiments were also fabricated. One set of samples was fabricated on .1 Ω cm n-type Si substrates, a second set was fabricated with varying Si-rich SiO_2 thicknesses in the range from 100 Å to 1000 Å, a third set was fabricated with varying SiO_2 thicknesses in the range from 150 Å to 500 Å (both thermally grown and CVD SiO_2 layers), and a fourth set was fabricated on an n-type degenerately doped poly-Si substrate with an n-type degeneratively doped poly-Si control gate.

Although R_o = 3 Si-rich SiO_2 material was used for the injectors in this study, R_o = 3 to 5 Si-rich SiO_2 materials could have also been used to get the same electrical injection characteristics when deposited on SiO_2. Also, Si-rich SiO_2 thickness is not very critical in at least the range from 100 Å to 500 Å for R_o=3 material. These aspects make the

material processing of devices using Si-rich SiO_2 layers very flexible, allowing desirable process tolerances needed for manufacturing.

B) Cross-Section TEM

Insulator and poly-Si stacks deposited on single crystal Si substrates similar to the DEIS MOSFETs used for the electrical studies but with thicker insulating layers for better resolution were fabricated for cross-section transmission electron microscopy (TEM) studies [41,42]. Figures 3-5 show cross-section TEM views of various regions of the device. Figure 3 shows an overall view up to the second poly-Si (gate electrode) layer. Figure 4 shows the gate oxide and floating poly-Si layer where clearly very planar, smooth interfaces (within the TEM's 10 Å resolution) between the thermally grown SiO_2 and the Si substrate and deposited poly-Si layers are seen. The second poly-Si layer used for the control gate looks very similar to the first layer of poly-Si. Figure 5 shows the DEIS stack which conforms to the rough bottom poly-Si surface. Asperities on this bottom rough poly-Si surface are $\approx$ 800 Å high and $\approx$ 1600 Å wide which are similar to those observed by Anderson and Kerr using SEM [17]. The interfaces between SiO_2 and Si-rich SiO_2 which are believed to control the electron injection phenomena, are distinguishable. The bottom interface appears to be somewhat rougher ($\lesssim$ 100 Å high ripples) than would be expected from conformal mapping of the underlying poly-Si surface. High resolution electron microscopy (HREM) currently in progress suggests a possible explanation for the difference in the interfaces is due to differences in atomic structure of the two Si-rich SiO_2 layers [43]. These observations could possibly explain the phenomena observed (discussed in section IV-B) on all DEIS stacks with equivalent Si-rich SiO_2 thicknesses and supposedly equivalent composition (including capacitors using smooth single crystal Si substrates and Al gate electrodes) which is that the bottom injector gives the same magnitude of current as the top injector at an SiO_2 average electric field magnitude which is smaller by 1.5-2 MV/cm. Surface roughness similar to that seen with cross-section TEM at the interface of the bottom Si-rich SiO_2 injector with the CVD SiO_2 was observed on a slightly larger scale with scanning electron microscopy (SEM) on the top surface of films of various thicknesses from 200 Å to 1000 Å deposited on single crystal Si with the size of the asperities decreasing with Si-rich SiO_2 thickness, but the shape remaining approximately constant. The DEIS stacks in Figs. 3-5 are thicker than normally used so that the interfaces between the various layers could be clearly resolved. Thinner DEIS stacks show similar behavior.

The grain size and surface roughness of the poly-Si layer was not changed drastically with annealing at 1000°C in N_2 for 30 min after deposition at temperatures between 650°C and 700°C. However, heavy $POCl_3$ doping and drive-in at 870°C of the poly-Si layers did have an effect on the poly-Si morphology. The undoped poly-Si layer shows small grain size next to its bottom (≈ 100 Å in size) with large columnar grains near its top (2,500 Å in size). Grain sizes of ≤ 500 Å were confined within the first 2,000 Å of poly-Si at which point a drastic increase in grain size is observed reaching the maximum very rapidly. In the poly-Si layers which were degenerately doped n-type with $POCl_3$, the grain size is on the average equal (≈ 900 Å in size) over the entire poly-Si layer thickness.

C) Measurement techniques

On the FET structures, the d.c. drain current as a function of gate voltage with 100 mV applied to the drain and with the source and substrate at ground potential was used to determine the transistor turn-on or threshold voltage, V_T. This in turn is a measure of the charge state of the floating poly-Si electrode (written, erased, or neutral). A low noise voltage ramp with adjustable ramp rates was used to supply the gate voltage and a Keithley model #610C electrometer was used to measure the electron current flowing from source to drain. This electrometer was operated with a 100 Ω resistance in series with the source to drain resistance. This 100 Ω resistor had less than 4% of the 100 mV applied to the drain dropped across it for the measurements performed here. Two Hewlett-Packard pulse generators (model #214A) were used to supply the write and erase voltages to the gate electrode. These write and erase pulses were usually equally spaced from one another with either a 25 msec or a 100 msec delay interval between them.

For the capacitor structures, currents flowing through the DEIS, SEIS, and control structures were measured using a Keithley model #26220 logarithmic picoammeter with a voltage source that had adjustable ramp rates. In all capacitor measurements, a virgin as-fabricated location was ramped from 0 V at rates of ± .5 V/sec or ±5 V/sec to the desired value. For measurements at positive ramp rates (negative ramp rates), white light was used to maintain the inversion layer in the p-Si (n-Si) substrate and prevent any significant voltage from being dropped across the Si. This white light, although shielded by the thick Al gate electrode, provides minority carriers electrons (holes) around the periphery of the depletion layer formed under the positively (negatively) biased Al electrode. These electrons (holes) subsequently diffuse laterally and form the inversion layer in the p-Si (n-Si) substrate.

IV. Results and Discussion

In the first part of this section (IV-A), the experimental results will be discussed for single injector structures using one Si-rich SiO_2 layer under the top, poly-Si control gate which writes under negative gate voltage by electron injection from this layer and erases under positive gate voltage using localized field enhancement from the top surface of the floating poly-Si charge storage layer. In the next part of this section (IV-B), dual injector Si-rich SiO_2 structures which use a Si-rich SiO_2 layer deposited above the floating poly-Si for erasing under positive gate voltage (see Fig. 2) will be discussed. In section IV-C, retention studies of DEIS, SEIS, and controls for temperatures from 25°C to 300°C and stressing gate voltages of 0 V, +4 V, or −4 V will be discussed and shown to be compatible with a 3 eV deep well for stored electrons on the floating poly-Si layer. Also reliability and voltage breakdown with single and dual electron injector structures as compared to the controls will be shown to be greatly improved in section IV-D.

A) Single Electron Injector Structure (SEIS)

As discussed in sections II and III-A, single injector FETs using a top Si-rich SiO_2 layer similar to the FET shown schematically in Fig. 2 and Fig. 6 without the bottom injector, were fabricated and tested. Using drain current as a function of gate voltage characteristics as shown in Fig. 7, threshold voltages V_T were deduced by extrapolating the experimental curves to 0 A drain current. For example, the virgin curve in Fig. 7 has a V_T value of 1.2 V. By comparing the value of V_T after putting electrons on (write) or taking them off (erase) the floating poly-Si layer (V_{T_f}) to the initial virgin value (V_{T_i}), the charge on the poly-Si floating gate can be determined from [44,45]

$$\Delta V_T = V_{T_f} - V_{T_i} = -Q_o\left[\frac{\bar{x}_o'}{\varepsilon_o} + \frac{\ell_n}{\varepsilon_n}\right] \tag{1}$$

where ℓ_n is the thickness for the SEIS or sum of thicknesses for the DEIS of the Si-rich SiO_2 layers, $\bar{x}_o'$ is the trapped charge centroid position (location of floating poly-Si) measured from the SiO_2–Si-rich-SiO_2 interface for the SEIS or the intervening oxide thickness (between Si-rich SiO_2 layers) for the DEIS, Q_o is the trapped charge per unit area on the floating gate, and ε_o and ε_n are the low frequency permittivity of the SiO_2 and Si-rich SiO_2 layers, respectively [13]. At the low voltages used in determining V_T, the Si-rich SiO_2 material is not very conductive and has a finite dielectric constant of $\approx$ 7.5 [12,13]. SiO_2 has a dielectric constant of 3.9. Therefore, $\varepsilon_o(\varepsilon_n)$ is given by 3.9(7.5) × the permittivity of free space which is

8.86×10^{-14} F/cm. The values of V_T on all virgin, as fabricated structures discussed in section III-A were always indicative of the floating poly-Si layer being in an approximately net neutral to slightly positively charged state initially. A slightly lower boron doping concentration of the Si substrate than that assumed here (4×10^{16} B atoms/cm^3 for 0.5 Ωcm p-type Si) could also be accountable for this calculated, slightly-positive initial charge state. Figure 7 shows that the drain current characteristic shifts in a parallel fashion to higher (lower) voltages when electrons are put on (taken off) the floating gate. Electrons are put on or taken off this charge storage layer using the top injector properties for writing and the field enhancement at the rough poly-Si surface for erasing.

After many write/erase cycles ($\approx 10^4$), the device becomes more difficult to write or erase. This is shown graphically in Fig. 8 which plots V_T as a function of the number of write/erase cycles for several write/erase control gate voltage, $V_{W/E}$, conditions where all voltage pulses are 5 msec in duration. The collapse of the write/erase window in Fig. 9 can be shown to be due to trapped electrons building up in the intervening SiO_2 layer between the floating and control gates. The internal electric field caused by this negative space charge build-up lowers the net field near the injecting interfaces (Si-rich-SiO_2–SiO_2 or rough polycrystalline Si-SiO_2) and therefore decreases the number of electrons that can be injected from the control gate to the floating gate or vice-versa to write or erase, respectively, the charge storage layer. An order of magnitude calculation for the capture cross-sections, $\sigma_{c_{ox}}$, for these traps can be performed using the relationships

$$\sigma_{c_{ox}} = \frac{q}{J_p \tau_{ox}} \tag{2}$$

[18] and

$$J_p = \frac{dQ_o}{dt} \tag{3}$$

where Q_o is determined from measured values of ΔV_T using equation 1, it is assumed that all injected electrons are stored on the floating gate, q is the charge on an electron (-1.6×10^{-19} coul), J_p is the magnitude of the particle current flow per unit area between the floating and control gate during write or erase operations, and τ_{ox} is the time constant associated with oxide charge trapping. Assuming that $\tau_{ox} \approx 2 \times \Delta t \times$ [number of cycles to pronounced window collapse ($\approx 10^4$ to 10^5 cycles)] where Δt is the write or erase pulse duration (5 msec) and using the time averaged value of J_p which is $Q_o \div \Delta t$, a value of $\sigma_{c_{ox}}$ in the range of 10^{-17} to 10^{-19} cm^2 is obtained. This is in the range of values found in the

literature for charge trapping in thermal SiO_2 or annealed CVD SiO_2 layers [13,18,19,46]. Figure 9 shows that these traps can be emptied thermally by annealing at 400°C for 20 min in forming gas. After annealing, the device cycles almost in the same manner as the virgin as-fabricated structure. This is again consistent with values for activation energies for thermal discharge of SiO_2 traps [18,46]. It is interesting that MNOS devices have window collapse also after $\approx 10^5$ cycles, and it has been speculated that this collapse is associated with degradation of the thin (25-30 Å) SiO_2 layer. The portion of the cycling characteristics in Figs. 7 and 8 for $< 10^4$ cycles is probably controlled by the details of residual, permanent space charge build-up in the Si-rich SiO_2 injector, itself, if any is present [12] and by the charge build-up in the oxide regions very near the Si regions in the Si-rich SiO_2 layers or very near the Si asperities of the rough floating poly-Si surface [15,16,47].

The assumption that J_p can be represented by a uniform current per unit electrode area for bulk SiO_2 electron trapping even though the actual carrier injection mechanisms are believed to be localized at the injecting interfaces has been justified in previous publications for larger area (.006 cm^2) capacitor structures using single [13] and dual [37] Si-rich SiO_2 injectors. The reasoning is that the Si islands in the Si-rich SiO_2 layers which inject carriers are very small ($\leq$ 50 Å) and densely packed for 46% atomic Si materials, and that the bulk SiO_2 traps "see" this injected current as approximately uniform because of the scale of their distance from the interfaces [13]. From the symmetry of the window collapse after 10^4 cycles in Figs. 8 and 9, the same reasoning seems appropriate for erasure of the charge storage layer using the asperities on the rough, floating poly-Si surface [2,3,15-17], although these asperities may be more widely spaced (see Figs. 3, 5, and section III-B).

The control devices for wafer run MDT-113 (labeled A and A′ - see section III-A) which contained just a 210 Å thick CVD SiO_2 layer between the floating and control poly-Si layers could not be written to threshold voltages much larger than the virgin, as-fabricated value ($\approx$ 1.2 V) for any of the write voltage pulse conditions of Fig. 7. However, these structures could be over-erased to negative V_T values indicating electrons could be removed from the degenerately n-doped, floating poly-Si layer leaving behind the ionized positive donor phosphorus atom impurities. This is consistent with the behavior observed for oxides grown or deposited above rough poly-Si surfaces [15-17,47] where asperities give localized electric field enhancement particularly for voltage bias conditions favoring electron ejection from the poly-Si surface (positive gate voltage). For negative voltage bias, some current enhancement from the top gate contact-oxide interface over that from a planar surface is expected because of conformal mapping of the thin deposited layers (see Figs. 3, 5, section III-B, and refer-

ences [16,47]). This enhanced electron injection is never as large as that observed from the asperities on the rough poly-Si surface [16,47].

The magnitude of the time-averaged particle current per unit area ($Q_o/\Delta t$) for writing the devices in Fig. 8 by means of the Si-rich SiO_2 injector was calculated using the data in this figure. These values of the particle current density for device MDT-113-C′ are plotted in Fig. 10 and compared directly to measured currents for large area (.006 cm^2) capacitor structures with similar Si-rich SiO_2 injectors (see section III-A). The comparison in Fig. 10 is good, and the expected current enhancement over control structures (no injectors present) is observed [12,13,37]. The electric fields used for the FET devices in Fig. 10 were obtained by taking the average value of the maximum and minimum spatially averaged electric fields, $\mathcal{E}_{1\ max}$ and $\mathcal{E}_{1\ min}$, respectively, in the intervening SiO_2 layer between the floating and control poly-Si layers during write operations. Because of the moderate voltages used during writing (or erasing of DEISs to be discussed in section IV-B) and the low resistivity of the Si-rich SiO_2 [8,9,31], the voltage drops across the Si-rich SiO_2 layers are approximately negligible [12,13,37] and the electric fields are given by [13, 48-50]

$$\mathcal{E}_{1\ max} = \frac{V_g - \Psi_s - \Phi_{ms}}{\ell_o} \tag{4}$$

and

$$\mathcal{E}_{1\ min} = \mathcal{E}_{1\ max} - \left(1 - \frac{\bar{x}_o'}{\ell_o}\right)\frac{Q_o}{\epsilon_o} \tag{5}$$

where Q_o is determined from measured values of ΔV_T using Equation 1, ℓ_o is the total SiO_2 thickness (the sum of the thermal oxide thickness between the single crystal Si substrate and floating poly-Si gate and the CVD oxide thickness between the floating gate and control gate), $V_g = V_w$ (the negative write voltage applied to the control poly-Si gate electrode), Ψ_s is the surface potential for the 0.5 Ωcm p-type Si substrate, and Φ_{ms} is the difference in work functions between the gate material (n-degenerate poly-Si) and the p-type single crystal Si substrate.

The values of $J_p(t)$ deduced from plots of Q_o as a function of time and using Eq. 3 ($J_p = dQ_o/dt$) over the 5 msec time interval for writing from an uncharged floating poly-Si state are shown in Fig. 11a. Also in Fig. 11a, J_p as a function of time for erasing a SEIS from an uncharged state is shown. Erasing SEIS structures using the rough top surface of the floating poly-Si was observed to be very sensitive to subtle inadvertent changes in the

processing from one device run to the next. For example, SEISs from wafer MDT-DIS2-C erased at electric fields in the intervening CVD SiO_2 layer which were $\approx$ 1.4 times larger than those for SEISs from wafer MDT-113-C'. Writing or erasing a device from the charge state of the opposite sign (for example, writing a SEIS from the erased state) only differs from Fig. 11a in the first .5 msec where currents are higher due to the enhanced fields caused by the opposite sign of charge initially on the floating poly-Si charge storage layer.

The approximation (i.e., $\bar{\varepsilon}_1 = [\int_o^{\Delta t} \varepsilon_1 dt] / \Delta t \simeq [\varepsilon_{1\ max} + \varepsilon_{1\ min}]/2$) for the time average of the electric field in the intervening CVD SiO_2 layer was shown experimentally to be fairly accurate (to within $\approx$ 5%). This was done by studying the charge build-up on the floating gate as a function of time in 0.5 msec intervals out to 5 msec and then calculating the corresponding electric field. This is plotted in Fig. 11b. Also, it was experimentally verified that the sum of ten 0.5 msec pulses gives to within 15% the same threshold voltage shift as one 5 msec pulse for both write and erase operations. The reduction in the particle current in Fig. 11a is consistent with the charge build-up on the floating poly-Si storage layer which in turn lowers the electric field ε_1 in the CVD SiO_2 layer. This is shown schematically for both write and erase operations in Fig. 6.

B) Dual Electron Injector Structure (DEIS)

The DEIS FET is shown schematically in Fig. 2. It contains two CVD Si-rich SiO_2 injection layers separated by CVD SiO_2 For all DEIS capacitors and FETs discussed here, both Si-rich SiO_2 layers were deposited under identical CVD conditions to contain 46% atomic Si and have the same thickness. However, as will be shown, the electrical injection characteristics are not identical. Figures 12-14 compare drain current as a function of gate voltage (which is an indicator of the charge state of the floating poly-Si layer) for DEISs, SEISs, and CVD SiO_2 controls for the MDT-DIS 2 series of FETs under different write and erase gate voltage conditions (V_W or V_E). For all data in these figures, an as-fabricated device was first written and then erased as indicated by the arrows. Several conclusions can be reached from Figs. 12-14 which are in general valid for all series of devices studied here (MDT-113, MDT-DIS 2, and MDT-DIS 3):

1.) The controls are not easily written for the V_W conditions used here (−25 to −35 V). Only at −35 V, a small amount of charge can be put on the floating poly-Si layer of a control FET.

2.) The SEISs write at lower voltages than the DEISs. This is due to a small voltage drop across the additional injector. If injector thicknesses are kept small compared to oxide thickness, the effect becomes very small.

3.) The DEISs erase at lower voltages than the SEISs. This is due to the bottom injector controlling the erase mechanism rather than the asperities on the rough, floating poly-Si.

4.) The DEISs have an electrical asymmetry for positive (erase) and negative (write) gate voltage conditions which is believed to be due to differences in the two Si-rich-SiO_2–SiO_2 interfaces. The bottom interface appears "rougher", based on cross-section TEM and SEM results discussed in section III-B, regardless of the substrate (smooth or rough) the CVD stack is deposited on.

Figures 15 and 16 show cycling data for single and dual electron injector structures of the MDT-DIS 2 FET series. These curves are similar to those in Fig. 8 for the single electron injector FETs of the MDT-113 series which have thicker thermal and CVD SiO_2 layers. Erasure of SEISs on wafer MDT-DIS 2-C required larger electric fields than those needed for erasure of the SEISs on wafer MDT-113-C′ due to variations in the rough top surface of the floating poly-Si layer (as discussed in section IV-A). However, both of these structures could be written with similar electric field magnitudes due to the reproducible injection characteristics of the Si-rich-SiO_2–SiO_2 interface of the top injector (see Fig. 10). Again threshold window collapse due to electron trapping in the CVD SiO_2 layer starts between 10^4 to 10^5 cycles.

Time-averaged particle current densities during writing as a function of the time-averaged oxide electric field were calculated for both single and dual injector FETs of the MDT-DIS 2 series as described in section IV-A. This is shown in Fig. 10. Fig. 11 shows the particle current density and electric field during a 5 msec write interval. Also, the time-averaged particle current density flowing during erase of a DEIS FET was calculated using the same equations as for writing (see Eqs. 1 and 3). This follows rather easily, if erasing from the initial uncharged state is viewed as positive particle injection from the control gate electrode under positive bias and subsequent capture by the floating poly-Si layer. Actually, electrons are being removed from the floating poly-Si to the control gate, leaving behind ionized donors. The agreement of the calculated oxide currents in the FETs with those

directly measured on large area capacitor structures is again good. Agreement between different device runs is good. Single injector FETs have higher currents under write conditions than DEISs at the same average oxide field, because of the additional small voltage drop across the bottom Si-rich SiO_2 injector which is neglected in the calculations. The DEIS FETs where the DEIS stack is deposited on a rough poly-Si surface, show the same electrical asymmetry between write and erase operations as the capacitors where the DEIS stack is deposited on smooth, planar single crystal (<100>) silicon substrates. This implies that the injection mechanism is controlled by the Si-rich-SiO_2–SiO_2 interfaces [12,13,37]. Although not plotted in Fig. 10, average particle currents during erasure of single injector FETs using the field enhancement of the rough floating poly-Si surface were calculated in a similar manner as the DEIS FETs. These calculated currents were of the same order of magnitude as those directly measured on large area capacitors with rough poly-Si surfaces prepared in a similar manner to those described here [16,47].

In order to test the limits of gate oxide thickness and the voltages required for writing and erasing the vertical double poly-Si structures, the MDT-DIS 3 series of devices were fabricated with a 100 Å SiO_2 layer between the Si substrate and the floating poly-Si layer. As seen in Fig. 17, these structures switch in 5 msec at voltages between 11 V and 16 V because less of the applied voltage is dropped across the thin 100 Å gate oxide compared to the other series of devices (MDT-113 and MDT-DIS 2 with gate oxide thicknesses of 435 Å and 290 Å, respectively). Figure 18 shows 2 μsec switching at voltages between 17 V and 23 V. These are the lowest voltages and fastest switching times of any EAROM devices reported with excellent retention characteristics as will be discussed in section IV-C. The writing and erasing voltages in Figs. 17 and 18 could be further reduced by about half if the control gate area is made small with respect to the floating gate area for the structure in Fig. 2. A smaller control gate area will give a smaller capacitance from the control gate to the floating gate as compared to the capacitance from the floating gate to the Si substrate. Therefore, a larger portion of the applied voltage will be dropped across the DEIS stack for this device as compared to structures with equal control and floating gate areas.

Fig. 10 shows that these structures of the MDT-DIS 3 series are still similar to the others in terms of the time averaged particle current flowing between the floating and control gates as a function of the time averaged oxide field in this region during writing and erasing, calculated as described in sections IV-A and IV-B. The small differences in Fig. 10 between MDT-DIS 3 and the other series of FETs is again due to the neglect of the voltage drop across the Si-rich SiO_2 layers of the DEIS which becomes more important as the total oxide

thickness (thermal and CVD) becomes comparable to or less than the total Si-rich SiO_2 thickness.

In the preceding discussions on the write/erase operation of the DEIS, SEIS, and control FETs, electron leakage from the floating poly-Si layer to the Si substrate when writing with negative gate voltages or to the floating poly-Si layer from the Si substrate when erasing with positive gate voltages was ignored. However if enough negative charge is put on the floating gate during writing, the internal electric fields near the floating poly-Si–thermal-SiO_2 interface will become large enough to eject a significant number of electrons off of the floating poly-Si storage layer to cause a saturation of the number of stored negative charges. Similarily during erasing, if enough positive charge (ionized donors) is left on the floating gate, the internal electric fields near the Si-substrate–thermal-SiO_2 interface will become large enough to inject a significant number of electrons on to the floating poly-Si storage layer to cause a saturation of the number of stored positive charges. This phenomenon will occur when the particle current injected from the top (bottom) Si-rich SiO_2 layer is approximately equivalent to the leakage current from the floating poly-Si layer to the Si substrate (from the Si substrate to the floating poly-Si layer) during write (erase) operation. The difference in the average electric fields in the oxide layers, defined as $\Delta\varepsilon_{2\rightarrow 1} = \varepsilon_2 - \varepsilon_1$ (CVD SiO_2 is layer 1 and thermal SiO_2 is layer 2), when the currents are approximately equal will give an estimate for the maximum number of stored charges possible before leakage becomes important through the relationship $Q_o = \epsilon_o \Delta\varepsilon_{2\rightarrow 1}$ [48-50]. For the write (erase) operation, the magnitude of $\Delta\varepsilon_{2\rightarrow 1}$ is $\approx$ 2.5 MV/cm ($\approx$ 4 MV/cm) which gives 5.4 x 10^{12} stored electrons/cm^2 (8.6 x 10^{12} ionized donors/cm^2). The magnitudes of $\Delta\varepsilon_{2\rightarrow 1}$ are deduced by comparing current–electric-field data such as those in Fig. 10 to those observed for injection via Fowler-Nordheim tunneling from a planar Si–thermal-SiO_2 interface [12,13,37]. The only case presented here where the floating gate might be over-charged is writing at -35 V for 5 msec the SEIS or DEIS FET's from the MDT-DIS 2 series. Trapped electronic charge build-up in the intervening CVD SiO_2 layer after 10^4 cycles will further increase the leakage to the Si substrate during writing to the same charge state of the floating poly-Si layer for $< 10^4$ cycles due to the increase in the electric field it causes near the poly-Si–thermal-SiO_2 interface and the subsequent increase in Fowler-Nordheim tunneling of electrons off the floating poly-Si layer to the Si substrate. Additionally, this negative trapped CVD SiO_2 charge decreases the field near the top injector Si-rich-SiO_2–SiO_2 interface and therefore decreases the injected particle current from the control gate.

As can be seen by comparing Fig. 8 with Figs. 15-18, threshold-voltage window collapse starts on all device series (MDT-113, MDT-DIS 2, MDT-DIS 3) after $\gtrsim 10^4$ cycles.

Values of $\sigma_{c_{ox}}$ for the oxide traps in the range of 10^{-17} to 10^{-19} cm^2 can be shown for all devices using the particle current densities in Fig. 10 and the procedure and equations previously described in section IV-A. These CVD oxide traps are bulk, uniformly distributed sites which are believed to be related to the water content in the SiO_2 layer [12,13,18,19,37,46]. Thinner oxide layers have a fewer number of total traps, but the same volume density. From the data of Fig. 16 (MDT-DIS 2) and Fig. 17 (MDT-DIS 3), the number of filled traps per unit area can be obtained. For example using the $V_g^- = V_w = -35$ V for 5 msec data in Fig. 16 for the write operation, $\Delta V_g^- = \Delta V_w \approx -5$ V is needed to return the device after $\gtrsim 10^5$ cycles to the operation it had at $\lesssim 10^4$ cycles. With the added -5 V, the field near the injecting interface (top Si-rich-SiO_2–SiO_2 interface for writing) and therefore the injected current density are returned to values they had prior to extensive charge trapping in the bulk of the CVD SiO_2 layer. Assuming the oxide trapped electron distribution is uniform which puts the centroid in the middle of the CVD SiO_2 layer (i.e., $\bar{x}'_{ox} \approx 75$ Å for MDT-DIS 2), the total number of filled traps per unit area, N_{ox}, can be calculated from the electrostatic relationship $N_{ox} = \varepsilon_o \Delta V_g^- (\ell_o - \bar{x}'_{ox})^{-1}/q$ (see Equation 5 and section IV-A). This calculation gives $\approx 3 \times 10^{12}$ filled traps/cm^2 with a volume density of $\approx 2 \times 10^{18}$ filled traps/cm^3. This filled trap volume density is ≈ 10 times larger than the total number of traps with similar capture cross section magnitudes observed for thermally grown SiO_2 films [19]. The density of these CVD SiO_2 traps could be further reduced by pre-annealing of DEIS stacks in forming gas or N_2 at high temperatures (700°C to 1000°C) [12,13,37] before the top poly-Si layer used for the control gate is deposited. However, smaller cross-section traps ($<10^{-19}cm^2$) could still limit the cyclibility of the EAROMs.

For the devices with the thin 100-150 Å CVD SiO_2 layers between the control gate and the floating poly-Si layers (MDT-DIS 3 and MDT-DIS 2), threshold-voltage window collapse saturates and levels off for $\gtrsim 10^5$ cycles. This apparent saturation of the threshold voltage window collapse is due to a slow down of the capture rate caused by the decrease in the particle current density as traps are filled and not due to the complete filling of <u>all</u> traps in this capture cross section magnitude range [18,19]. This was shown by a recycling experiment. Using a device (MDT-DIS 2-B) which was cycled to obtain the data in Fig.16, the threshold voltage window was reopened by increasing V_W from -35 V to -40 V and V_E from +27.5 V to +36 V. With these new $V_{W/E}$ voltages, the FET showed a very similar cycling characteristic with a similar threshold-voltage window collapse after $\approx 10^4$ cycles. However, the details of the threshold-voltage window collapse were different, with the erase portion of the window remaining open about an order of magnitude more cycles. Periodically during the

recycling experiment, the gate voltage of the first cycling sequence ($V_{W/E}$ = −35 V and +27.5 V) were applied to show that the threshold voltage window was still collapsed. This was done to check that trapped electrons in the CVD SiO_2 layer were not being removed (via electric field ionization) by the larger bulk oxide fields caused by the increase in the write/erase voltages needed for the recycling experiment.

For all the cycling measurements discussed previously, the write and erase pulses were equally spaced from each other by 25 msec or more. For pulse-spacing times less than 25 msec, space charge effects in the Si-rich SiO_2 injectors, particularly in the DEIS FETs, had a noticeable effect on the cycling data. This phenomenon occurs because electrons still remain in the opposite non-injecting si-rich SiO_2 layer [12] from the previous write or erase pulse since a sufficient delay time has not been allowed for this charge to move back to the control or floating poly-Si gate electrode. This electronic charge which is probably trapped in the Si regions of the Si-rich SiO_2 layer produces an electric field which opposes electron injection from the opposite Si-rich-SiO_2–SiO_2 interface by lowering the electric field near it. This effect can be minimized by decreasing the response time for electron movement out of the injectors back to the appropriate poly-Si electrode. Response time decrease could be obtained by increasing the Si content of the Si-rich SiO_2 layers, thereby increasing its conductivity, and/or decreasing the Si-rich SiO_2 thicknesses (50-100 Å would be the minimum value still consistent with good injector current enhancement [12]) so as to minimize both the distance over which trapped electrons in the Si-rich SiO_2 layer have to move to get back to the contact and the amount of trapped charge itself which therefore effects the electric fields. The effect on the oxide field near the opposite Si-rich SiO_2 injector due to these trapped charges can also be minimized by increasing the intervening CVD SiO_2 thickness, but this would also increase write/erase voltages for a given structure. Space charge effects in the injecting Si-rich SiO_2 layer itself of a SEIS or DEIS FET could also become noticeable for very short write/erase pulse lengths due to the finite time involved for the movement of electrons from the contact to the Si-rich-SiO_2–SiO_2 interface via the Si islands. Also, this space charge trapped in the Si-rich SiO_2 layer could affect the electronic injection from the contacts if it builds up near the contact–Si-rich-SiO_2 interface rather than moving rapidly to the Si-rich-SiO_2–SiO_2 interfacial region.

C. Charge Retention

Charge retention studies were performed after charging the floating gate of DEISs, SEISs, or control structures to levels of ≈ 3-5 × 10^{12} charges (electrons or ionized donors)

/cm^2 at temperatures of 25°C, 100°C, 200°C, and 300°C with stressing voltages of 0 V or ± 4 V. The DEISs and SEISs were charged with electrons by means of the top Si-rich SiO_2 injector while the controls were charged from the single crystal Si substrate using optically induced hot electron injection [51]. The control and SEIS can be put in a positive charge state (erased) by means of enhanced fields near the rough floating poly-Si top surface while the DEIS was erased by means of the bottom Si-rich SiO_2 injector. In general, as will be shown here, the retention of negative charge was controlled by the ≈ 3 eV depth from the bottom of the SiO_2 conduction band to the Fermi level of the degenerate n-doped floating poly-Si layer or to the conduction band bottom of the Si islands in the bottom Si-rich SiO_2 layer of the DEIS and the local electric fields with or without Si-rich SiO_2 injectors present.

Figure 19 shows a plot of the ratio of the threshold voltage shift after retention stressing to that before stressing ($\Delta V_T(t)/\Delta V_T(0)$) as a function of stressing time at V_g = 0 V and temperatures of 25°C, 100°C, 200°C and 300°C for DEIS, SEIS and control devices from the MDT-DIS 2 series of samples. Devices from the MDT-113 or MDT-DIS 3 series also behaved in a similar fashion. As seen in this figure, no charge loss (i.e., < 25 mV) is observed for 25°C or 100°C. At 200°C and 300°C, some loss is seen after ≈ 10^5 sec and ≈ 10^4 sec, respectively. All three types of structures behave similarly at a given temperature. Discharging is entirely controlled by thermal activation out of a 2.2 eV deep well with .2 eV broadening assumed. With no broadening, the well is 2 eV deep. This is shown schematically in Fig. 20a using an energy band diagram. The activation energy for the case of no broadening was calculated from first order kinetics assuming a frequency factor s = 10^{12} sec^{-1} (which is the order of magnitude of atomic vibration frequencies), a single trapping energy level associated with electrons in the conduction band of the floating poly-Si layer or in the conduction band of the Si islands in the bottom Si-rich SiO_2 layer of the DEIS, and negligible retrapping of discharged electrons [52]. With these assumptions, it can be shown that

$$\frac{\Delta V_T(t)}{\Delta V_T(0)} = \exp\left[-st \exp\left(-E_a/kT\right)\right] \qquad (6)$$

where t is the time is sec, k is Boltzmann's constant, T is the absolute temperature, and E_a is the single level activation energy. If .2 eV broadening is included in the calculation with Equation 6 modified accordingly [52] to account for the n-type degeneracy of the poly-Si (Fermi level is ≈ .2 eV above the bottom of the poly-Si conduction band edge) and to possibly account for the disordered nature of the Si-rich SiO_2 material system, the activation energy from the bottom of the SiO_2 conduction band edge to the energetic center of the poly-Si well or the wells of the Si islands is 2.2 eV. This value is still less than the expected

energy depth of ≈ 3 eV [18]. However, if Schottky barrier lowering [45] due to the internal fields generated by the trapped negative space charge itself (which amounts to ≈ .4–.6 eV for the highest local internal fields) [13, 48-50, 53] is taken into account, the actual thermal depth becomes ≈ 2.6 - 2.8 eV for zero electric field conditions which is reasonably close to the expected depth. The highest internal oxide fields for the devices in Fig. 19 are located locally near the rough poly-Si surface asperities with the CVD SiO_2 layer (between floating and control gates) in the control and single injector structures or probably near the interface of the last layer of Si islands in the CVD Si-rich SiO_2 with the CVD SiO_2 layer in the DEIS [13, 48-50, 53]. Also, optical detrapping measurements [18,50,53] of electrons trapped on floating poly-Si layers performed on similar capacitor structures with semi-transparent Al gate electrodes, verified the expected optical depth of 3 eV. From Equation 6, it can easily be shown that for electrons in a 2 eV deep well at temperatures from 25°C to 80°C only 5% of the initial charge will be lost over times $> 10^{15}$ sec (3×10^7 yrs.) by thermal activation. Similar retention data to that in Fig. 19 were also observed on devices which were written with electrons after having been cycled $\gtrsim 10^6$ times and then annealed at low temperatures ($\lesssim$400°C) to remove the trapped electrons in the intervening CVD SiO_2 layer. If the trapped electrons in the intervening CVD SiO_2 layer are not removed by annealing, the retention for electrons on the floating poly-Si storage layer should be increased. This is due to the trapped electrons in the CVD SiO_2 layer lowering the electric field near the bottom Si-rich-SiO_2–SiO_2 interface for the DEIS or near the rough poly-Si–CVD-SiO_2 interface for the SEIS and control.

The Si-rich SiO_2 layer because of its highly non-ohmic conductivity and ability to build-up trapped space charge will give an increasingly more probable conduction path to its interface with the CVD SiO_2 layer with increasing electric field for electrons on the floating poly-Si [8,9,31]. Conduction through the Si-rich SiO_2 for 46% atomic Si is believed to be due to tunneling between the Si regions [12]. Internal photoemission and photoconductivity measurements under negative gate bias conditions on Al and Au contacts to Si-rich SiO_2 layers deposited on top of SiO_2 suggest that the bottoms of the conduction bands of the Si regions are also energetically ≈ 3 eV deep from the bottom of the SiO_2 conduction band [12].

Activation of mobile Na^+ ions out of SiO_2 traps near the Si-SiO_2 interface [54] and the subsequent movement of these ions to the floating poly-Si layer under the influence of the internal electric field of the trapped electrons where the Na^+ ions could compensate some of this negative space charge can not explain the data of Fig. 19. Since thermally activated mobile Na^+ release near Si-SiO_2 interfaces occurs at temperatures $\lesssim$ 150°C [54], trapped

electron compensation by these ions should be readily seen within 10^5 sec at temperatures $\lesssim$ 200°C. This was not observed.

If positive voltages are applied during the charge retention measurements, the discharge rate of the trapped electrons can be increased somewhat, particularly for the DEISs. These losses are primarily due to Fowler-Nordheim tunneling at the Si-rich-SiO_2–SiO_2 interface (injector on top of floating poly-Si) [12,13,37] in addition to the thermal discharge over the potential barrier of the trapping well. This is shown schematically in Fig. 20b using an energy band diagram. The retention characteristics for V_g = +4 V at T = 300°C in Fig. 21 show that the SEISs and control structures behave similarly to the V_g = 0 V conditions of Fig. 19 which are dominated by thermal activation, and the DEISs show enhanced loss compared to Fig. 19 due to the additional tunneling. Calculation of the electric fields in the intervening SiO_2 layer of the DEIS for the V_g = +4 V and 4 x 10^{12} electrons/cm^2 case of Fig. 21 are consistent with expected losses due to tunneling (see Fig. 10). Also, the weak temperature dependence between 25°C and 300°C of the additional charge loss of the DEIS FET biased at +4 V in Fig. 21 is consistent with that expected for electronic Fowler-Nordheim tunneling out of the Si wells into SiO_2 at the Si-rich-SiO_2–SiO_2 interface over this same temperature range [12]. As charge is removed from the floating poly-Si, the internal fields will decrease, field dependent barrier lowering effects will lessen, and the discharge rate of any of the structures will slow down. If a device is read at +4 V in $\lesssim 10^{-6}$ sec, which is typical [5], a total of 10^8 times in one day for 10 years, it will have been cumulatively stressed approximately the same amount of time ($\gtrsim 10^5$ sec) as used here. Since reading is done at temperatures $\lesssim$ 80°C, read perturb effects will be negligible (see Figs. 19 and 21).

Retention measurements were also performed on the "erased" state of the SEIS and DEIS FETs at V_g = 0 V, +4 V, and −4 V at 300°C. Here ionized donors in the floating poly-Si layer form an attractive potential well for electrons injected from either the single crystal Si substrate or the top poly-Si gate contacts. This is shown schematically in Fig. 22 using energy band diagrams. Figure 23 shows the decrease in the number of ionized donors as a function of time on a DEIS FET at 300°C for gate voltage biases of 0 V, +4 V and −4 V. Little compensation of the total number of positive charges ($\approx$ 4 x 10^{12} donors/cm^2) is seen at 0 V and +4 V. This would be controlled mostly by thermal activation of electrons from near the bottom of the Si conduction band of the substrate Si contact, top poly-Si gate contact, and/or the Si islands in the top Si-rich SiO_2 injector probably near the Si-rich-SiO_2–SiO_2 interface into the SiO_2 conduction band and the subsequent movement of these electrons in the electric field to the floating poly-Si layer where ionized donors are then

compensated. This activation energy should again be $\approx$ 3 eV at zero electric field. However, the discharge of trapped electrons from the floating poly-Si layer via thermal activation (see Fig. 19) seems more pronounced than donor compensation by thermal activation from the Si contacts or top Si-rich SiO_2 injector (see Fig. 23, V_g = 0 V and +4 V data). This is probably due to the detailed differences in the local electric fields and their subsequent effect on barrier lowering near the appropriate Si layer or layer of Si islands in the Si-rich SiO_2.

At V_g = −4 V a decay is observed in Fig. 23 due to electronic Fowler-Nordheim tunneling from the top Si-rich SiO_2 injector as predicted from calculated electric fields. Again, this decay is not very temperature dependent (comparing 25°C and 300°C data for a DEIS FET at V_g = −4 V in Fig. 23) which is consistent with electronic Fowler-Nordheim tunneling at the upper injector Si-rich-SiO_2–SiO_2 interface [12]. These electrons are subsequently captured on the floating poly-Si layer. SEIS and DEIS FETs behaved similarly in all measurements since the top Si-rich SiO_2 injector, in particular, and the Si substrate, to a certain degree, controlled donor compensation by the number of electrons they injected. However, trapped electrons (see Fig. 19) are discharged faster for V_g = +4 V from the floating poly-Si layer of DEIS FETs than an equivalent number of ionized donors are compensated at V_g = −4 V (see Fig. 23) because of the different Fowler-Nordheim tunneling efficiencies for the bottom and top Si-rich SiO_2 injectors (bottom injector is more efficient, see Fig. 10).

For long times involving months or years ($> 10^6$ sec), the discharge rate of the DEIS FETs (for positive or negative stored charge) or SEIS FETs (for positive charge) at room temperature will be controlled by electronic Fowler-Nordheim tunneling at the Si-rich-SiO_2–SiO_2 interfaces. Electrons will tunnel off the floating gate to the control gate by means of the bottom injector for stored negative charge. For stored positive charge, electrons will tunnel from the control gate to the floating gate by means of the top Si-rich SiO_2 injector. Charge retention studies were performed on DEISs and control structures from the MDT-DIS 2 and MDT-DIS 3 series of FETs for 3-5 x 10^{12} stored electrons/cm^2 over many months with the devices stored on the shelf at room temperature with the control gate floating. The electronic charge losses for the DEIS were slightly larger than for the controls, but these losses were $\lesssim$ 10% of the total charge initially stored with most of the charge loss occuring over the first few months. This demonstrates that the charge loss is self-limiting since as the electric fields which drive the loss process are lowered by the leakage of the stored charge, further loss of charge is decreased. A similar phenomenon was observed for large area SEIS EAROMs with a tungsten ("W") trapping layer for charge storage [12] (instead of poly-Si). Here the charging rate of initially empty W traps by the single top Si-rich SiO_2 injector at low applied

negative gate voltages was observed to slow down rapidly after the first few hours [12]. The trapping rate continued to decrease over weeks, and only a small amount of charge was put into the still nearly empty W traps. It was argued that the trapped electronic space charge build-up in the top Si-rich SiO_2 layer and its internal field were the cause of the decrease in the trapping rate by limiting the supply of electrons injected from the top Al gate contact [12].

If the Si-rich SiO_2 injectors of the DEIS or SEIS FETs are much thicker than the intervening CVD SiO_2 layer, these devices may have better retention characteristics than the control structures depending on the amount of time the Si-rich SiO_2 appears to be an insulator with a dielectric constant of $\approx$ 7.5. This would be controlled by the amount of time it takes for space charges from the poly-Si control gate or floating gate to fill up the Si-rich SiO_2 injectors, cause a collapse of the electric field to a low value in these layers, and thereby force most of the voltage to be dropped across the intervening CVD SiO_2 layer. However, if most of the voltage is dropped across the much thicker Si-rich SiO_2 regions (at least initially), then the oxide fields near the Si-rich-SiO_2–SiO_2 interfaces would be much lower than in the oxide layer of the control. Also, fewer carriers might be present for injection into the SiO_2 layer when thick Si-rich SiO_2 injectors are present due to limitations on the motion of carriers through the Si-rich SiO_2 region after injection from the contacts.

D. Breakdown and Reproducibility

In this section, DEISs will be shown to have very few low voltage breakdowns compared to control structures with no Si-rich SiO_2 injectors present. This phenomenon is believed to be due to the reversible space charge build-up in the Si-rich SiO_2 layers at low applied voltages [12]. Here electrons injected from the contacts into the Si regions in the Si-rich SiO_2 layer are confined to this layer by the blocking, highly resistive, intervening SiO_2 at low voltages where tunneling into the SiO_2 is not very probable. These trapped electrons reduce the electric field in the Si-rich SiO_2 layer. A space charge will build up next to any portion of the contacting Al, single crystal Si, or poly-Si area whose surface gives locally high fields and therefore large injected currents [36]. These localized areas of high fields are believed by many to be a leading cause of <u>low</u> voltage breakdowns in MOS structures. Previous publications have demonstrated this concept where high local fields were created by asperities on a rough poly-Si surface [16,17]. Charge trapping on purposely added "W" sites $\approx$ 70 Å from this rough poly-Si – SiO_2 interface were used to screen the locally high electric

fields which caused high injected currents and therefore breakdown at low applied voltages [47].

Figures 24 and 25 demonstrate that very few low voltage breakdowns are observed on DEISs. In Figs. 24a and 25a, about a hundred DEIS capacitors with an area of .006 cm^2 discussed in section III-A (single crystal Si – 200 Å Si-rich-SiO_2 with R_o = 3 – 400 Å SiO_2 – 200 Å Si-rich-SiO_2 with R_o = 3 – Al) are ramped from 0 V under negative gate voltage bias conditions at a rate of 1.25 MV/cm-sec (−5 V/sec) to current levels of 2×10^{-6} A (Fig. 24a) and then to 5×10^{-4} A (Fig. 25a), sequentially. All histograms (Figs. 24 and 25) use .5 MV/cm bins. These figures show that very few low voltage breakdowns occur, and they are representative of the electrical reproducibility across the 1¼ inch wafers. This electrical reproducibility, which is the voltage or average field in the SiO_2 layer necessary to draw a particle current of either 2×10^{-6} A or 4×10^{-4} A, is consistent with the CVD SiO_2 thickness variation (≈ 10%) across the wafers due to the flow patterns in the CVD reactor used. Even for currents as high as 5×10^{-4} A (≈ .1 A/cm^2), the histogram of Fig. 25a is not characteristic of voltage breakdown, but only of reproducibility of injected currents from the Si-rich SiO_2 injector under the Al gate electrode.

Figures 24b and 25b show that the control structures (single crystal Si – 400 Å CVD SiO_2 – Al) have many low voltage breakdowns occurring due to the absence of the Si-rich SiO_2 injectors. Clearly, after the first ramped cycle to a current level of 2×10^{-6} A, all of the capacitors are leaky or have broken down. The second cycle to 5×10^{-4} A, breaks down all of the remaining capacitors.

Histograms yielding similar conclusions to those in Figs. 24 and 25 were also observed on SEISs and controls fabricated on n-type Si substrates and ramped at positive gate voltages (+5 V/sec). Here the single Si-rich SiO_2 injector is inbetween the Si substrate and the SiO_2 layer rather than inbetween the gate electrode and the SiO_2 layer as described in section IV-A. The Si-rich SiO_2 injector on top of the Si substrate of the SEIS or just the substrate Si-SiO_2 interface of the control structure determines the breakdown characteristics observed. The substrate type, whether p-Si or n-Si, was chosen for negative or positive voltages, respectively, so that the Si substrate was always strongly accumulated during the ramped voltage measurement and no significant voltage was dropped across it.

Histograms yielding similar conclusions to those in Figs. 24 and 25 were also observed for DEIS capacitors with Si-rich SiO_2 injector thicknesses varying from 100 Å to 1000 Å and for the controls; for DEISs, SEISs, and controls with various SiO_2 thicknesses in the range

from 150 Å to 500 Å; for SEISs and controls with thermal SiO_2 layers rather than CVD SiO_2; and for DEISs and controls sandwiched between n-degenerate poly-Si contacts for either voltage polarity. Also, control structures which had identical processing compared to the wafer in Figs. 24b and 25b but no 1000°C anneal in N_2 for 30 min. prior to metallization (see section III-A) had better voltage breakdown histograms because of the H_2O content of the CVD SiO_2 layer and the charge trapping associated with it [47].

This section demonstrates that devices using DEIS stacks to charge or discharge floating poly-Si structures as opposed to only SiO_2 layers as done with the newest EAROMs [2,3,14] are less likely to be effected by contact controlled low voltage breakdowns. Chip yields, based on electrical performance, for structures employing DEIS stacks should be much greater than those employing only SiO_2.

V. Conclusions

A new non-volatile memory using a floating poly-Si storage layer and a series of stacked insulators consisting of top and bottom layers of Si-rich SiO_2 and an intervening layer of SiO_2 between this floating poly-Si and a poly-Si control gate has been discussed. This device has been shown to give the cyclibility and low power of MNOS plus the charge retention and density of FAMOS. In addition, it has been shown to operate at moderate gate voltages and moderate average oxide electric fields. The dual electron injector structures used in this EAROM demonstrate the use of "insulator engineering" to achieve the desired write and erase characteristics of this memory, independent of each other and independent of the read operation which uses electric fields at the thermal-SiO_2–substrate-Si interface. Future uses of DEIS stacks with or without faster switching times may be in the area of non-volatile random access memory (NVRAM), particularly as a back-up memory for data storage in case of a power failure or shut-down.

The simple physical model presented here allows accurate determination of write, erase, and retention characteristics. This model uses the bottom of the conduction band of the floating poly-Si storage layer or the Si islands in the Si-rich SiO_2 layers at an $\approx$ 3 eV depth with respect to the bottom of the SiO_2 conduction band, and it uses the enhanced current injection phenomena occurring at Si-rich-SiO_2–SiO_2 interfaces (see Fig. 10). Previous publications have shown that the Si-rich-SiO_2 used here (46% atomic Si) has at least two phases (Si and SiO_2) [31-35] which probably cause the local electric field distortion and current enhancement at the interfaces due to the size, shape and density of the Si regions [12,13,36]; that when injecting significant numbers of electrons into the SiO_2 layer, the Si-rich

SiO_2 is highly conducting with respect to the SiO_2, but at low fields it behaves more like an insulator with a dielectric constant of 7.5 which builds up a reversible space charge [12,13]; and that the bottom of the conduction band of the Si regions in the Si-rich SiO_2 layers are also $\approx$ 3 eV deep from the bottom of the SiO_2 conduction band [12].

Other insulator combinations, such as Si-rich Si_3N_4, and Si_3N_4 may prove useful for certain device applications where two carrier enhanced injection is required [11,29]. For DEIS stacks sandwiched between metal lines made of materials like Al, low temperature plasma-enhanced CVD materials may be advantageous.

ACKNOWLEDGEMENTS

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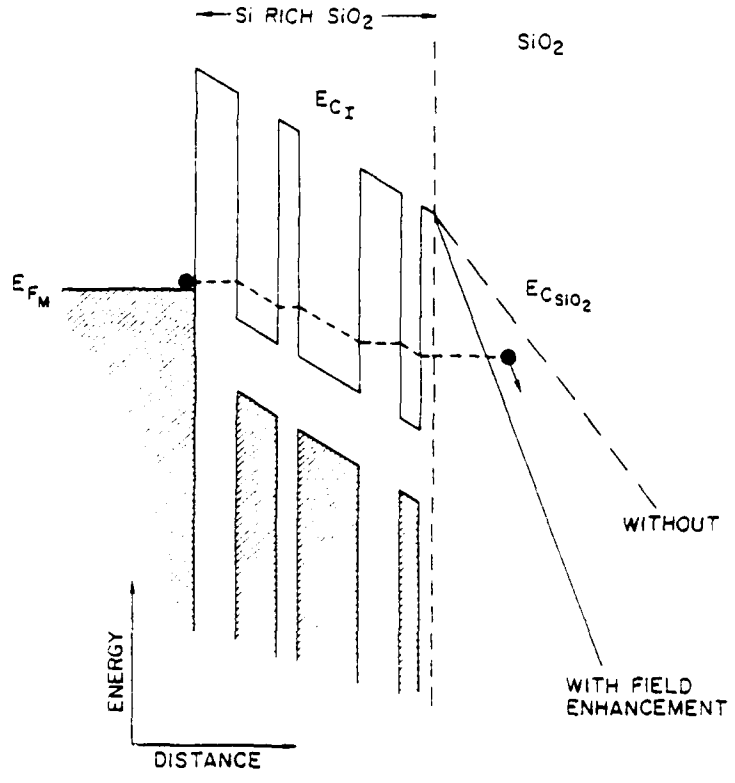

Figure 1. Schematic band representation of the electronic conduction in the Si-rich SiO_2 layer via direct tunneling between isolated Si regions in the SiO_2 matrix of this two phase system and subsequent high field injection into the underlying SiO_2 region due to local electric field distortions caused by the curvature of the Si regions.

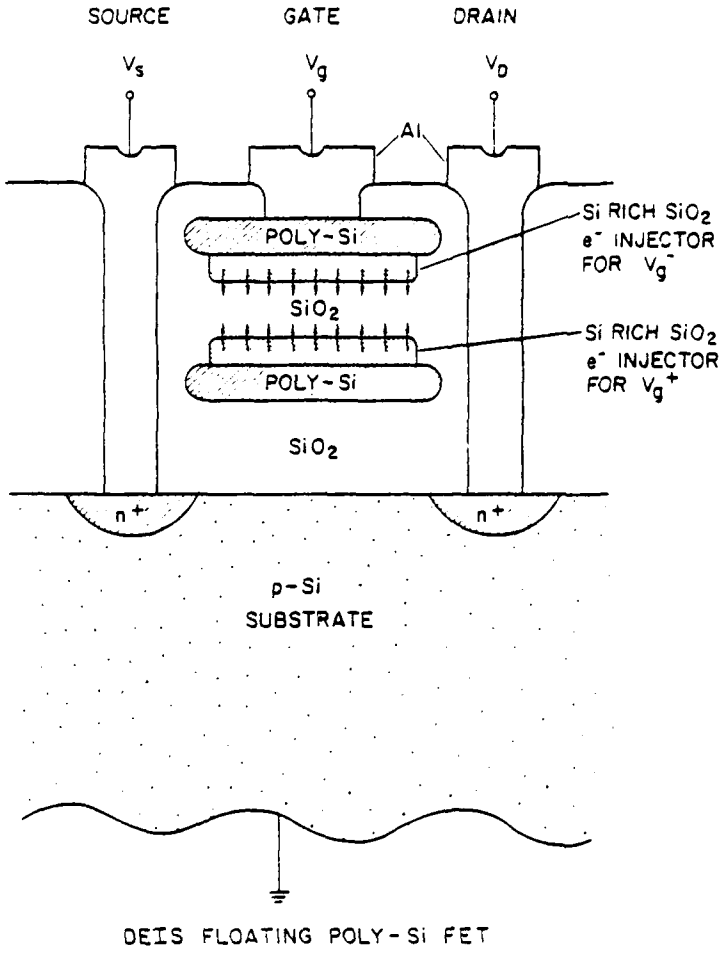

Figure 2. Schematic representation of a non-volatile n-channel field effect transistor memory using a dual electron injector stack between a control gate and a floating poly-Si layer. Writing (erasing) is performed by applying a negative (positive) voltage, Vg^- (Vg^+), to the control gate which injects electrons from the top (bottom) Si-rich SiO_2 injector to the floating poly-Si storage layer (back to the control gate). Structure is not drawn to scale.

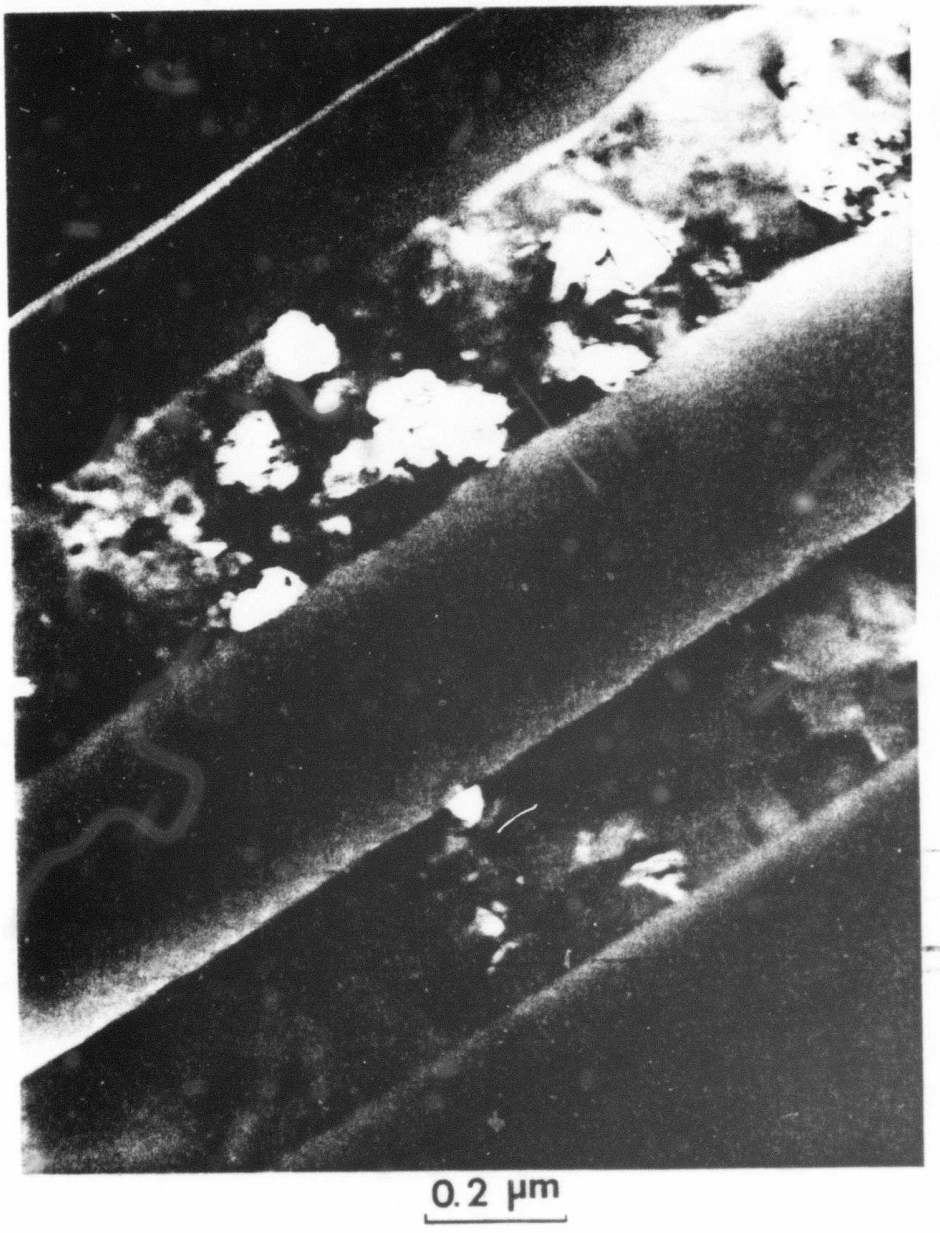

Figure 3. Dark-field cross-section TEM of total stacked structure depicted in Fig. 2. Poly-Si layers have been doped degenerately n-type with a $POCl_3$ diffusion at 870°C.

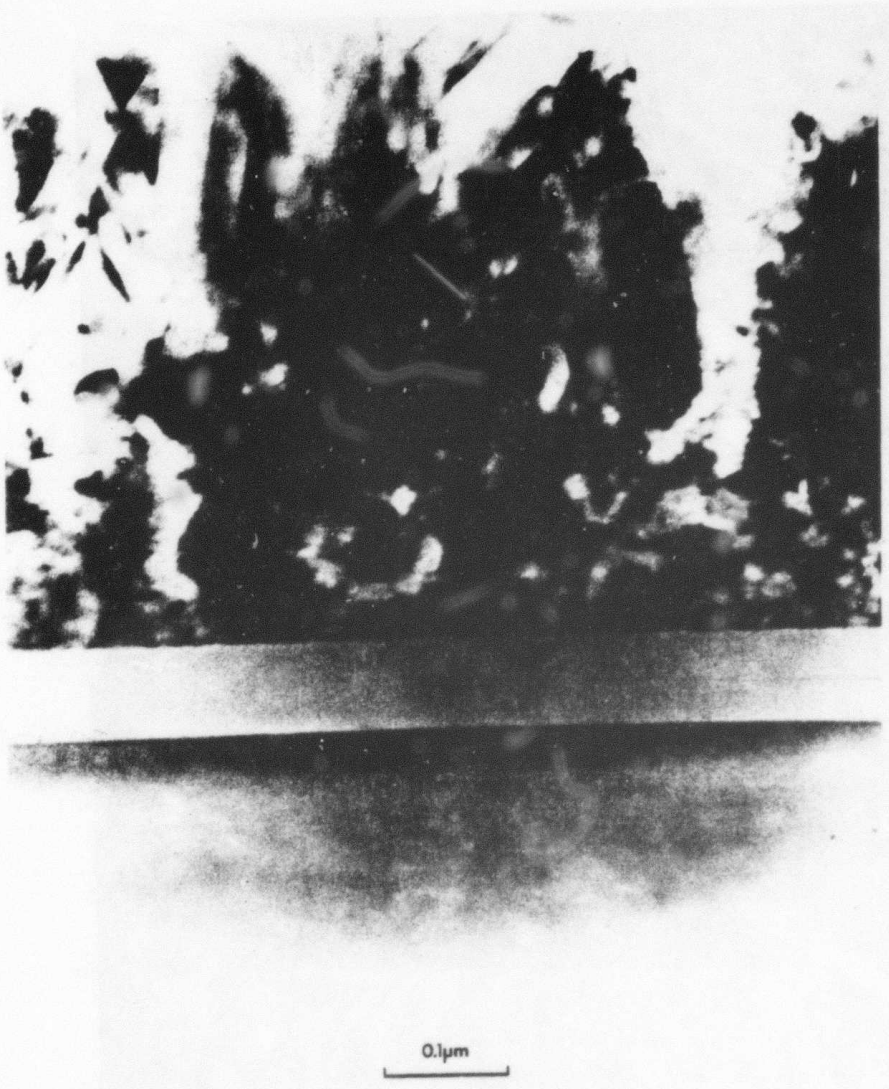

Figure 4. Bright-field cross-section TEM of the top part of the Si substrate, thermal gate SiO_2 layer, and the lower part of the first poly-Si layer (floating storage layer). Poly-Si layers are undoped.

Figure 5. Bright-field cross-section TEM of DEIS stack on top of the first (floating) poly-Si layer with lower part of top (control gate) poly-Si layer showing in uppermost part of the micrograph. Poly-Si layers are undoped.

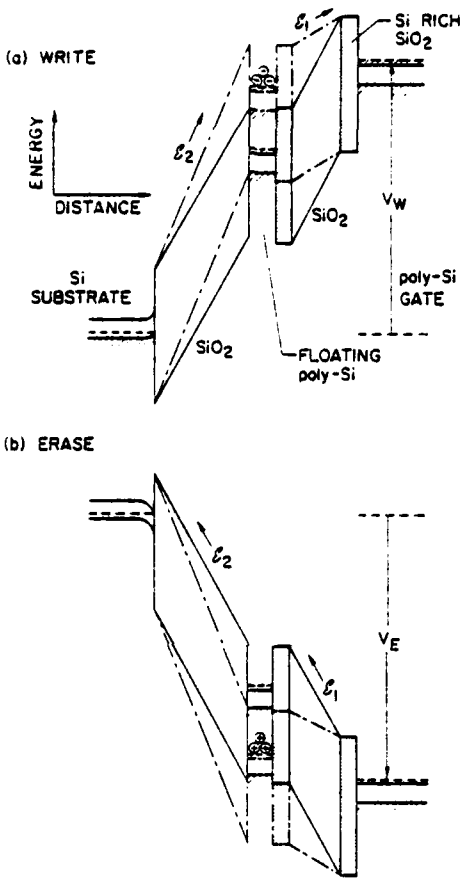

Figure 6 Schematic energy band representation of an FET using Si-rich SiO_2 injectors for (a) writing and (b) erasing a floating poly-Si charge storage layer. Solid and dot-dash lines represent the uncharged and charged (either (a) negatively or (b) positively) EAROM, respectively. $\mathcal{E}_1$ and $\mathcal{E}_2$ indicate the average electric fields in the CVD and thermal SiO_2 layers, respectively.

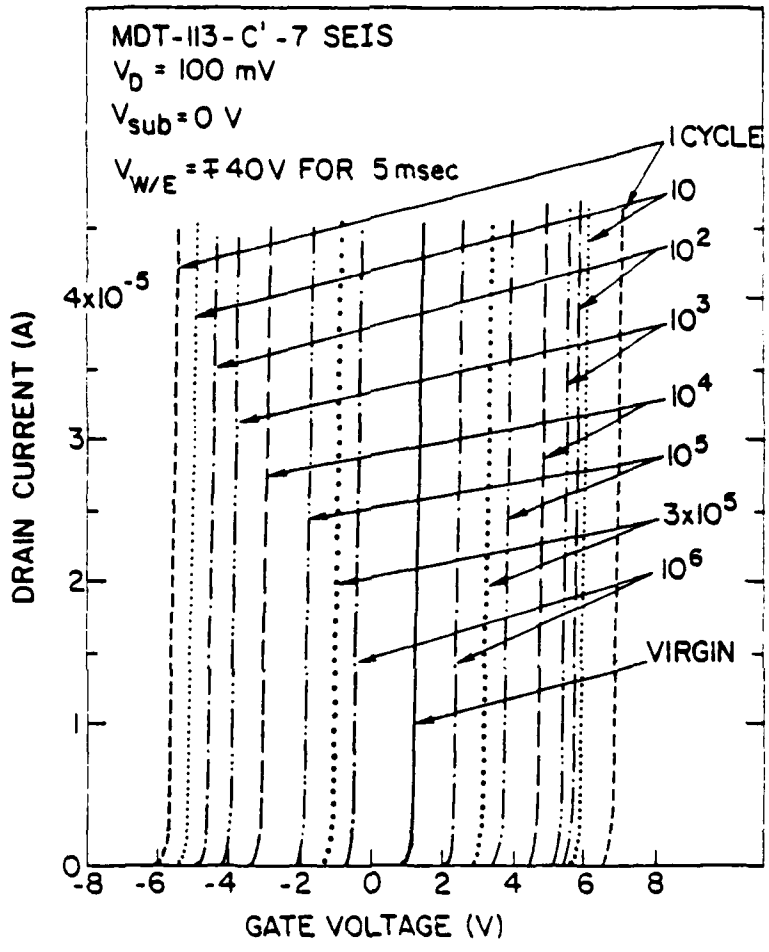

Figure 7. Drain current as a function of the gate voltage with the drain biased at V_D = 100 mV and the source and substrate grounded $V_S = V_{sub} = 0$ V. A SEIS FET from wafer MDT-113-C′ which was first written from its virgin uncharged state was then cycled as indicated with write and erase voltages of $V_g = V_{W/E} = \mp$ 40 V for 5 msec.

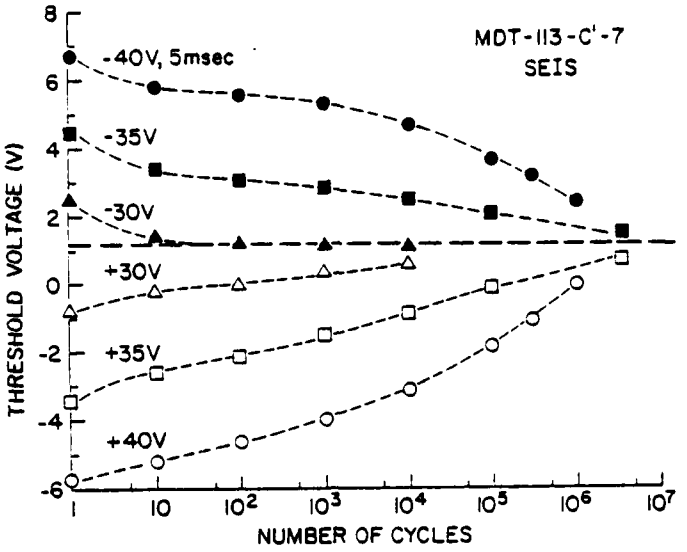

Figure 8. Threshold voltage after writing and erasing as a function of the number of write/erase cycles for various $V_{W/E}$ conditions on devices like those in Fig. 7. Solid and open symbols correspond to the threshold voltage after writing and erasing for 5 msec, respectively. The horizontal dashed line indicates the initial threshold voltage of the as-fabricated FETs before cycling.

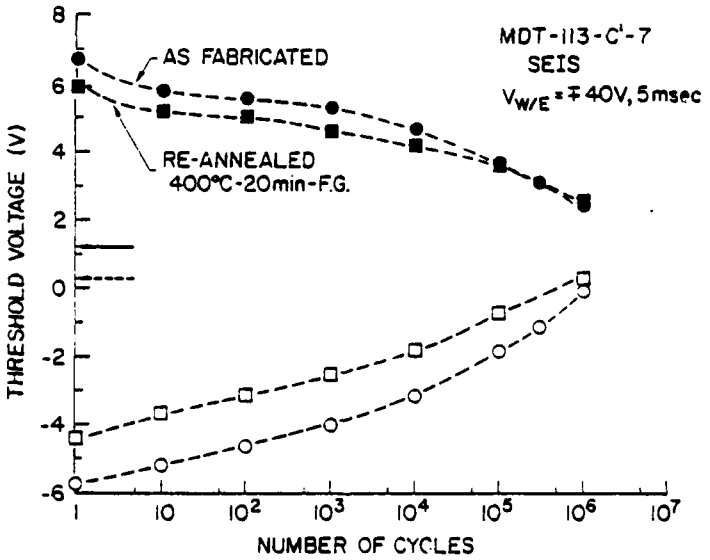

Figure 9. Threshold voltage after writing and erasing as a function of the number of write/erase cycles for the device in Fig. 7 as-fabricated, and after 10^6 cycles and re-annealing at 400°C for 20 min in forming gas to remove trapped electrons in the CVD SiO_2 layer which caused the collapse of the threshold voltage window. Solid and open symbols correspond to the threshold voltage after writing and erasing for 5 msec, respectively. The solid and dashed arrows indicate the initial threshold voltage of the as-fabricated and re-annealed FET, respectively, before cycling.

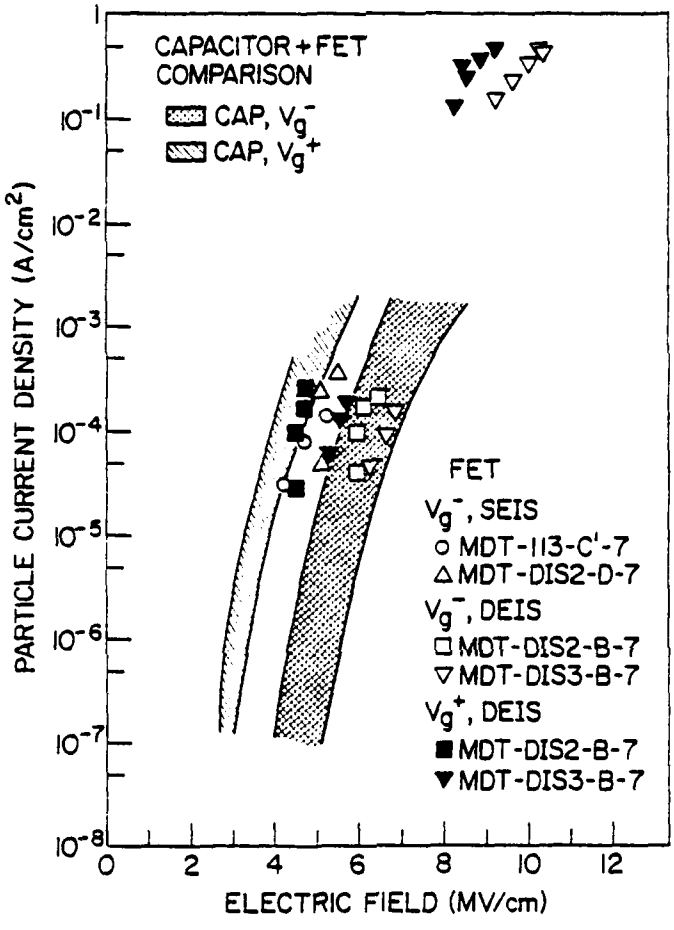

Figure 10. Comparison of the electronic particle current density as a function of the electric field for the oxide layer in DEIS and SEIS stacks incorporated into large area capacitors with smooth single crystal Si and Al contacts and small area FETs with poly-crystalline Si electrodes.

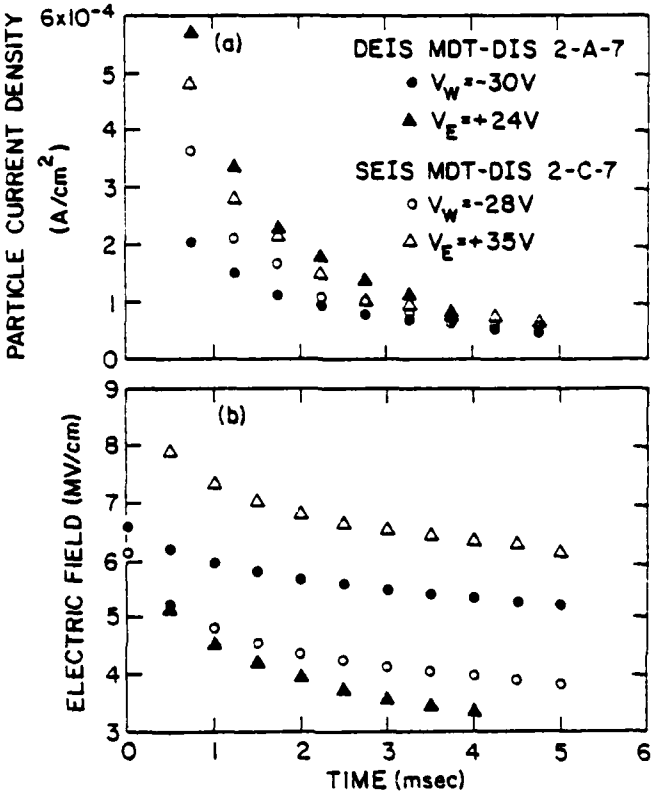

Figure 11. Electronic particle current density (a) and the corresponding electric field in the intervening CVD SiO_2 layer (b) as a function of time during a write or erase pulse of 5 msec for DEIS and SEIS FETs from the MDT-DIS 2 series.

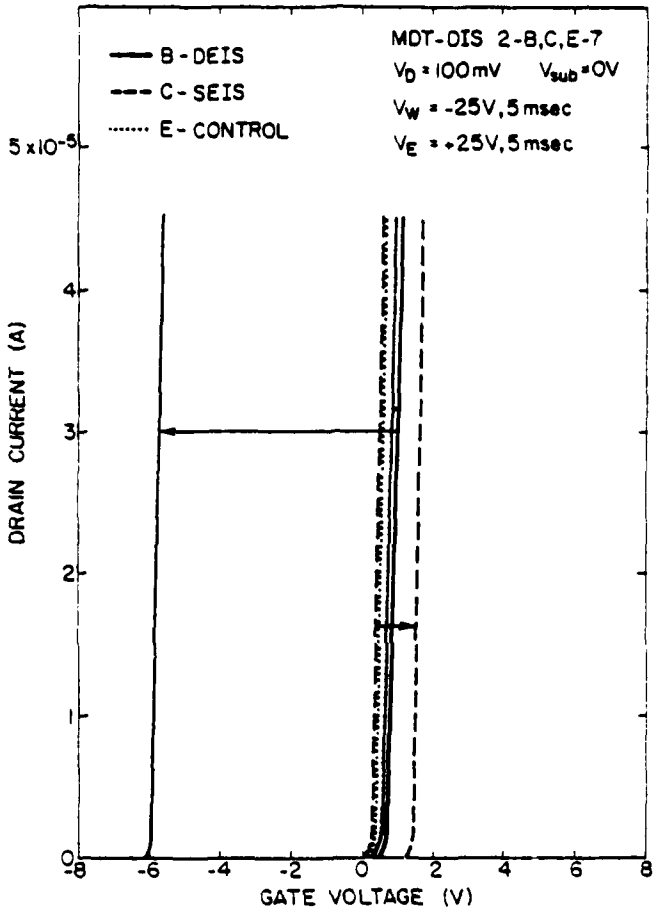

Figure 12. Comparison of the drain current as a function of the gate voltage under similar conditions as in Fig. 7 for DEIS, SEIS, and control FETs from the MDT-DIS 2 series. Each series of characteristics shows the behavior of the structure as it is first written with $V_W = -25$ V for 5 msec from the virgin as-fabricated state and then erased with $V_E = +25$ V for 5 msec.

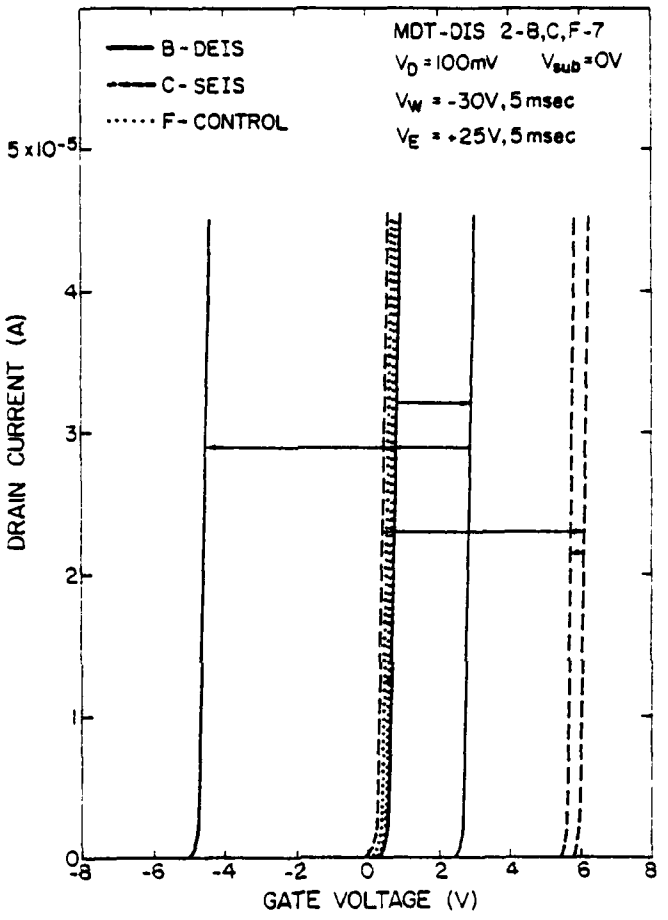

Figure 13. Comparison of the drain current as a function of the gate voltage under similar conditions and for a similar series of devices as in Fig. 12 but with $V_W = -30$ V.

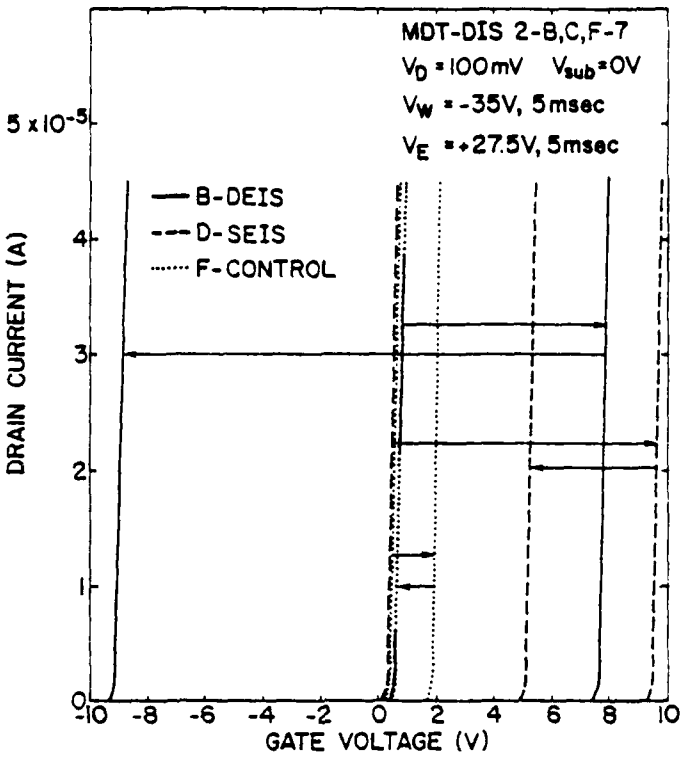

Figure 14. Comparison of the drain current as a function of the gate voltage under similar conditions and for a similar series of devices as in Fig. 12 but with $V_W = -35$ V and $V_E = +27.5$ V.

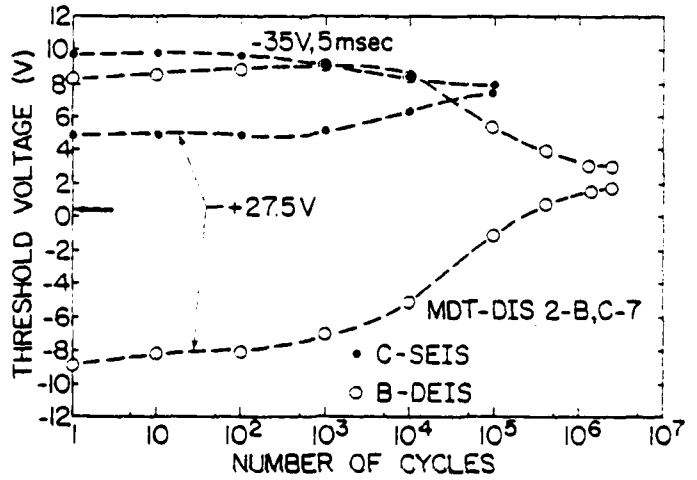

Figure 15. Threshold voltage after writing and erasing as a function of the number of write/erase cycles for a similar series of DEIS and SEIS FETs as in Fig. 12 under similar conditions. The solid and dashed arrows indicate the initial threshold voltage of the SEIS and DEIS, respectively, before cycling.

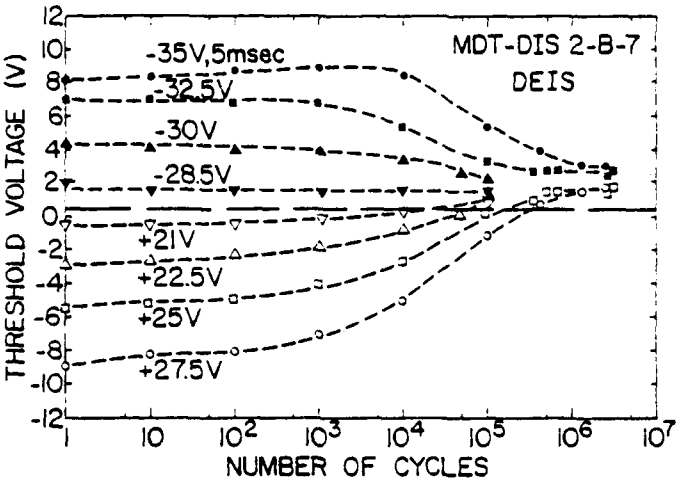

Figure 16. Threshold voltage after writing and erasing as a function of the number of write/erase cycles for various $V_{W/E}$ conditions on DEIS FETs from wafer MDT-DIS 2-B. Solid and open symbols correspond to the threshold voltage after writing and erasing for 5 msec, respectively. The horizontal dashed line indicates the initial threshold voltage of the as-fabricated FETs before cycling.

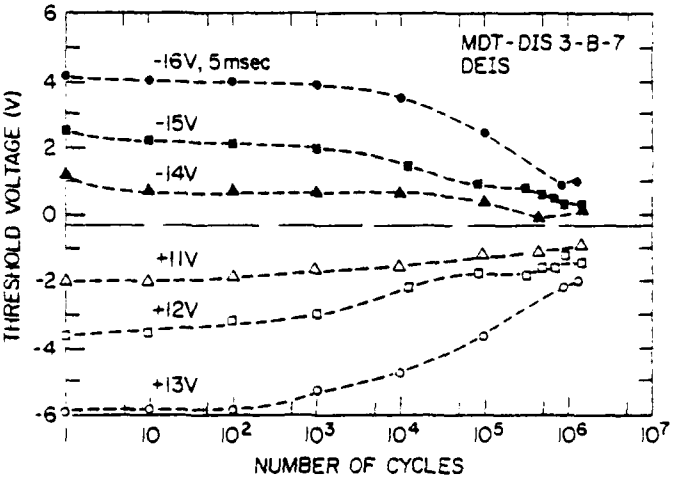

Figure 17. Threshold voltage after writing and erasing as a function of the number of write/erase cycles for various $V_{W/E}$ conditions on DEIS FETs from wafer MDT-DIS 3-B. Solid and open symbols correspond to the threshold voltage after writing and erasing for 5 msec, respectively. The horizontal dashed line indicates the initial threshold voltage of the as-fabricated FETs before cycling.

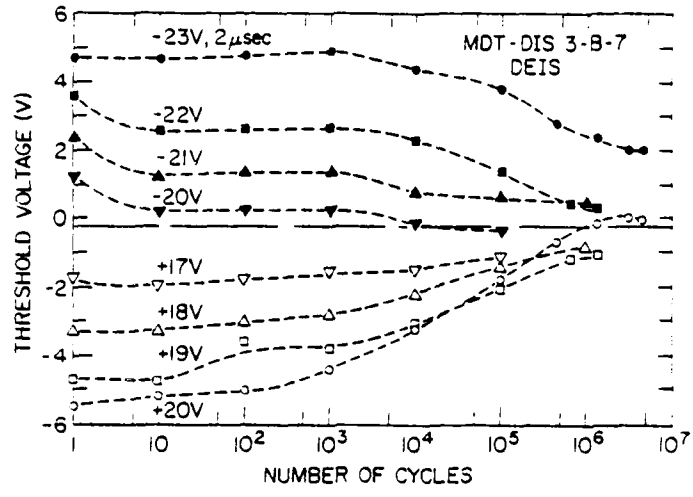

Figure 18. Threshold voltage after writing and erasing as a function of the number of write/erase cycles for various $V_{W/E}$ conditions on DEIS FETs from wafer MDT-DIS 3-B. Solid and open symbols correspond to the threshold voltage after writing and erasing for 2 μsec, respectively. The horizontal dashed line indicates the initial threshold voltage of the as-fabricated FETs before cycling.

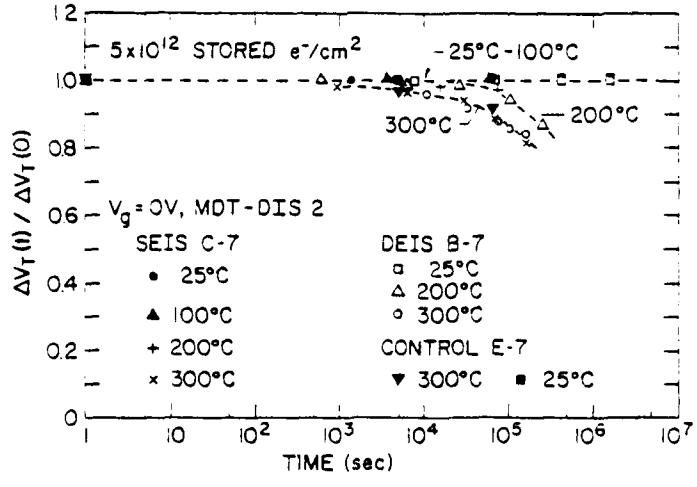

Figure 19. Stored electronic charge (initially ≈ 5 × 10^{12} cm^{-2}) loss as a function of time on DEIS, SEIS, and control FETs from the MDT-DIS 2 series for a grounded gate condition V_g = 0 V at temperatures of 25°C, 100°C, 200°C, and 300°C. Charge loss is calculated in normalized units of $\Delta V_T(t)/\Delta V_T(0)$ as described in the text.

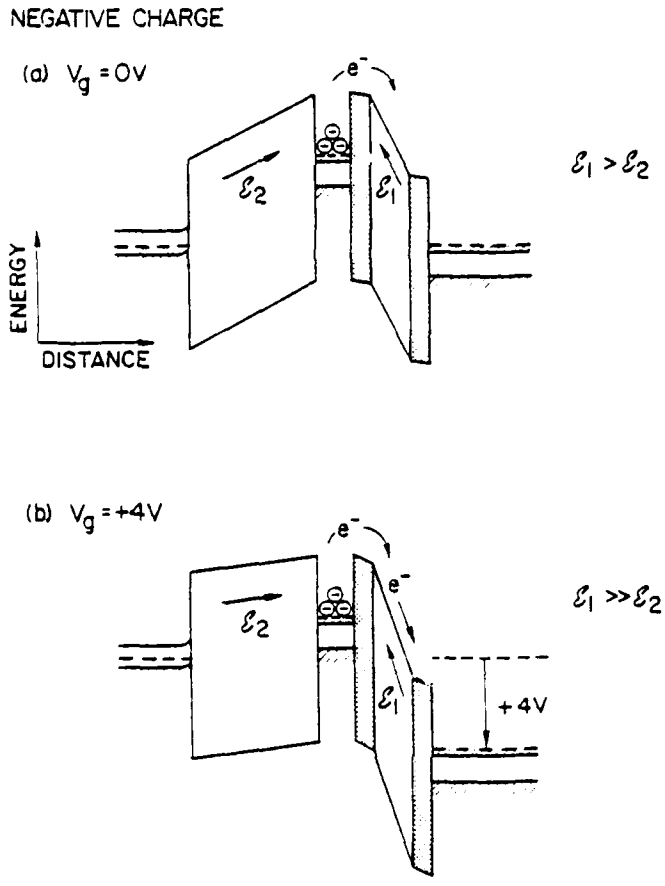

Figure 20. Schematic energy band representation of a DEIS FET with stored negative charge (electrons) on the floating poly-Si layer for (a) V_g=0 V and (b) V_g=+4 V gate voltage conditions. Notation is the same as in Fig. 6. Curved arrows indicate thermal discharge of electrons off of the floating poly-Si storage layer and the straight arrow indicates additional charge loss by Folwer-Nordheim tunneling.

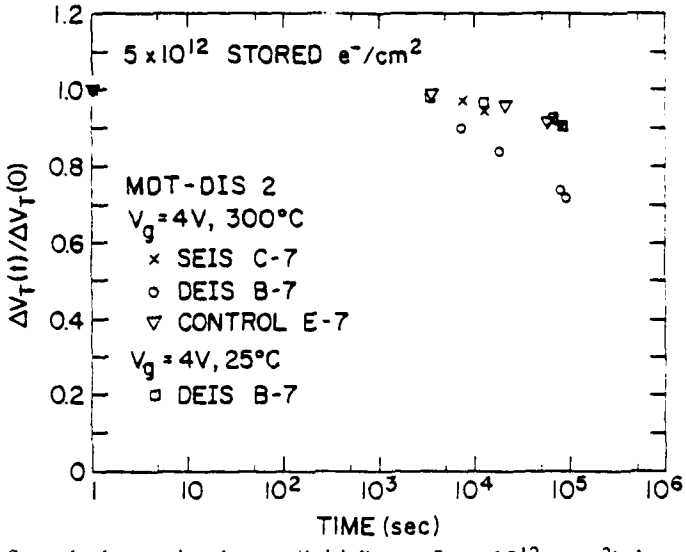

Figure 21. Stored electronic charge (initially $\approx 5 \times 10^{12}$ cm^{-2}) loss as a function of time on devices similar to those in Fig. 19 with $V_g = +4$ V at 25°C and 300°C. Same normalization as in Fig. 19 was used.

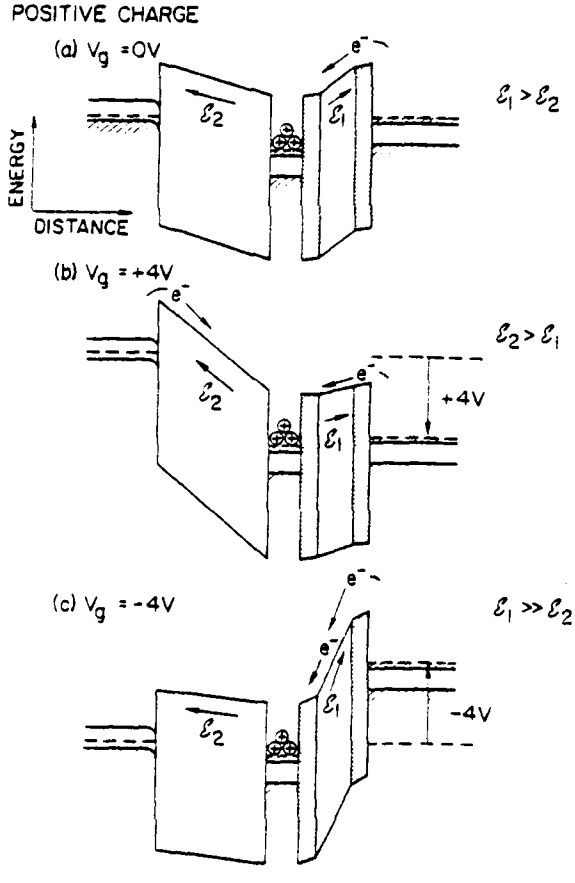

Figure 22. Schematic energy band representation of a DEIS FET with stored positive charge (ionized donors) on the floating poly-Si layer for (a) V_g=0, (b) V_g=+4 V, and (c) V_g=-4 V gate voltage conditions. Notation is the same as in Figs. 6 and 20.

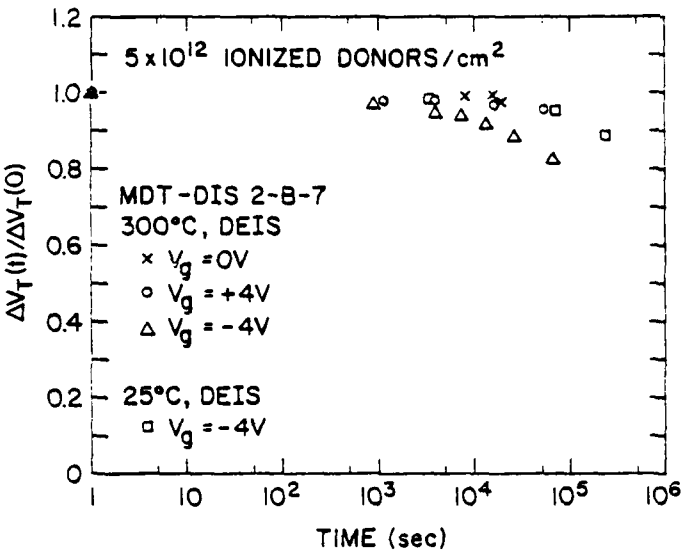

Figure 23. Stored positive charge (initially $\approx 5 \times 10^{12}$ cm^{-2}) loss as a function of time on devices similar to those in Fig. 19 for V_g = 0 V, +4 V, and −4 V at 25°C and 300°C. Same normalization as in Fig. 19 was used.

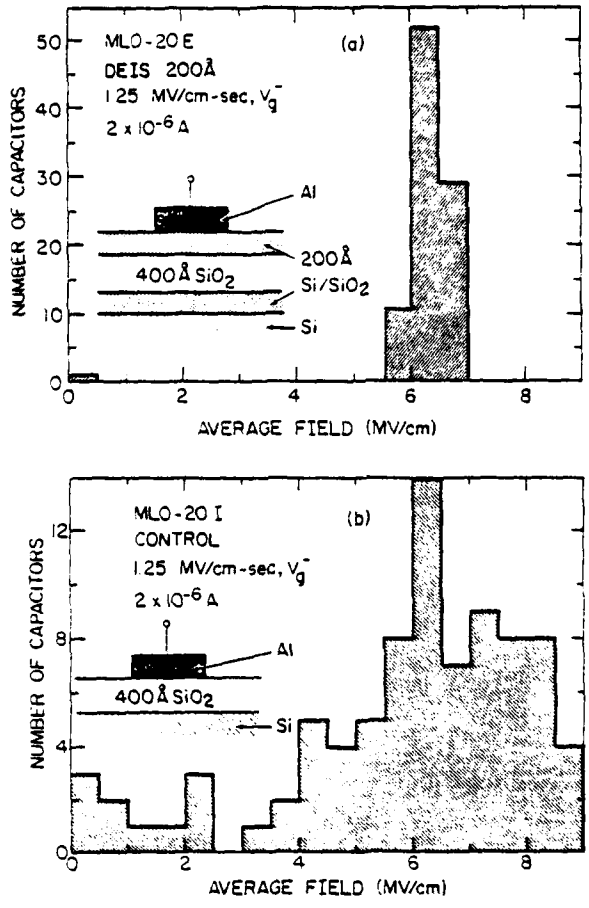

Figure 24. Histogram in 0.5 MV/cm bins of the number of capacitors (.006 cm^2 area) (a) on a DEIS wafer and (b) on a control wafer to draw a current of 2×10^{-6} A as a function of the average field in the 400 Å thick intervening CVD SiO_2 layer. Si-rich SiO_2 injectors were 200 Å thick and contained 46% atomic Si. Samples were ramped with negative gate voltage bias from 0 V at a rate of 1.25 MV/cm-sec.

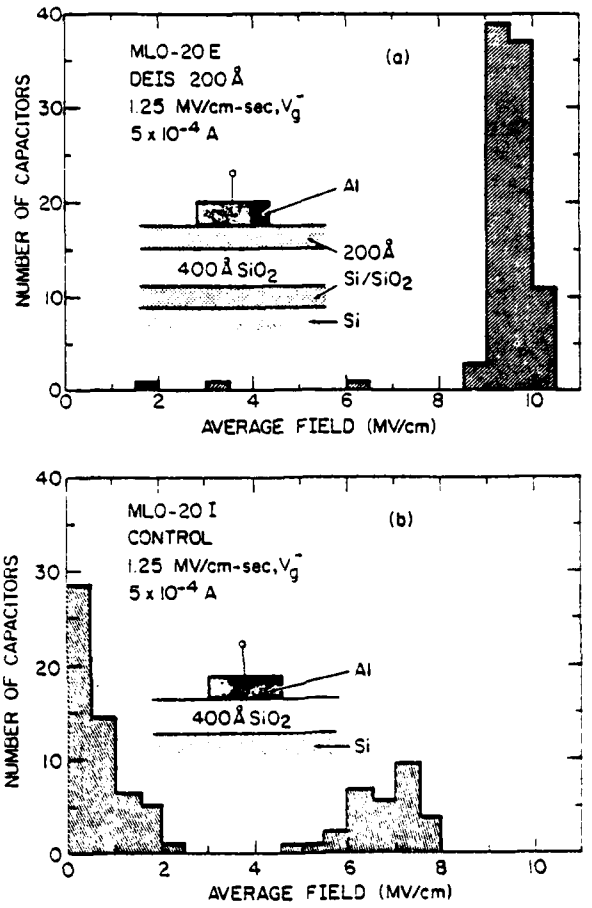

Figure 25. Histogram of the number of capacitors (a) on the same DEIS wafer and (b) the same control wafer as in Fig. 24 to draw a current of 5×10^{-4} A as a function of the average field, sequentially performed after first ramping to 2×10^{-6} A as shown in Fig. 24. Same experimental conditions as in Fig. 24 were used.

IDENTIFICATION OF ELECTRON TRAPS IN THERMAL SILICON DIOXIDE FILMS

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ABSTRACT

The infrared absorption of thermal SiO_2 has been measured using the attenuated total reflectance technique. The samples were subjected to various water diffusion and annealing treatments. Electron trapping was also measured in similar samples. The infrared measurements shows the presence of SiH, SiOH and H_2O groups in the SiO_2 films, particularly after H_2O diffusion. Examination of both the infrared absorption results and the electron trapping results show that the electron trap with a cross section of 1×10^{-17} cm^2 is associated with SiOH groups, and that the electron trap with a cross section of 2×10^{-18} cm^2 is associated with H_2O.

Numerous papers[1-5] have appeared recently describing the nature of electron trapping in SiO_2 and relating some of the traps to water in the SiO_2. The work primarily involved electrical measurements of the trapping, from which the trapping cross sections and the trap densities could be determined. From the photo I-V technique[6] one can learn the location of the traps in the oxide as well. In this letter we report measurements of the infrared absorption of thermal SiO_2, and correlate the observed impurities in the SiO_2 with water related trapping levels. In this way the microscopic identification of some of the trapping sites in SiO_2 can been made.

Pliskin[7] has investigated the infrared absorption properties of thick SiO_2 films deposited in a variety of ways. Of particular interest to us, he has correlated the strengths of the infrared absorptions due to SiOH and H_2O groups in these films to the concentrations of these impurities. Beckmann et.al.[8] and Murau et.al.[9] have used the attenuated total reflection (ATR) technique to look at the infrared absorption due to SiOH, H_2O and SiH groups in thin (< 1000 Å) SiO_2 films. Hartstein et.al.[10] have studied the impurities in CVD deposited SiO_2 and in doing so developed a quantitative experimental method for utilizing the ATR technique for SiO_2 films. This method has been used in the present experiments.

The samples used in this study were thermally grown SiO_2 films on Si total internal reflection elements. The oxides were dry thermal oxides grown at 1000 C for about one day. The samples were immediately placed in dry N_2

and allowed to cool in the N_2 atmosphere. They ranged in thickness from 2000 Å to 3400 Å. The infrared spectra of the films were measured, and the films were subjected to various H_2O drifting and dry annealing conditions. Water was diffused into the samples by annealing at either 250 C or 300 C in a H_2O environment. The technique used for this is similar to that used by Nicollian et. al.[11] Dry anneals in both N_2 and forming gas (F. G., a 10% mixure of H_2 in N_2) were performed at temperatures ranging from 300 C to 1000 C. Following any such sample treatment the infrared spectrum was remeasured.

The infrared spectra were obtained using a Perkin Elmer Model 180 spectrometer. The internal angle of incidence in the silicon total internal reflection element was 25°, and the geometry was such that 108 internal reflections were obtained. Fig. 1 and Fig. 2 show the infrared spectra obtained in two frequency regions for an SiO_2 sample which had water diffused in at 300 C. The film shows absorption lines at 3640, 3400 and 2260 cm^{-1}. The lines at 3640 cm^{-1} and 3400 cm^{-1} have been attributed to SiOH and H_2O groups, respectively.[7,10] The line at 2260 cm^{-1} has been attributed to the SiH group.[8,9,10]

The quantitative determination of the numbers of impurities giving rise to a particular absorption line in an ATR experiment has been described in detail by Hartstein et. al.[10] and will only be summarized here. First, the absorption strength of a known SiO_2 line is measured in a thick sample. The identical

line on a similarly prepared thin sample on the Si internal reflection element is also measured. The comparison between the two directly calibrates the absorption strength in the ATR geometry being used. The relationship between the absorption strengths of the 3640 cm^{-1} and 3400 cm^{-1} lines and the SiOH and H_2O content of the SiO_2 film was determined gravimetrically by Pliskin.[7] The relationship between the absorption strength of the 2260 cm^{-1} line and the SiH content was estimated by Brodsky et. al.[12] using a nuclear analysis. By combining these results we obtain the concentration of SiOH, H_2O and SiH in the films. It is very difficult to assess the accuracy of the absolute numbers determined in this way. The source of the possible errors come from the correlation of the infrared absorption to the impurity concentration. Any shifts in oscillator strengths between the calibration samples and our samples will introduce an error in the scale factor. This effect is probably not worse than a factor of 2. Nevertheless, since the uncertainty is in the scaling factor, the ratios of the concentrations are still known quite accurately, with an estimated error of $\pm 10\%$.

Table 1 gives the densities of the observed impurities in two samples as they were subjected to a number of sequential processing steps. The numbers were determined from the observed infrared absorption using the analysis which was described above. Sample 1 was 3400 Å thick and grown in an ultradry environment. Sample 2 was 2000 Å thick and grown in a less carefully controlled dry environment. Therefore, the initial impurity concentra-

tions in the two samples are different. Nevertheless, some general observations about the data can still be made. The SiOH content of the samples increases markedly following H_2O diffusions. The actual H_2O content may either increase or decrease as a result of the H_2O diffusion step. Following a subsequent annealing treatment, in either N_2 or F. G., the SiOH content is decreased, but at the same time the H_2O content is increased. This strongly suggests a conversion of OH to H_2O without the need for additional H_2. A long time anneal eventually diffuses the H_2O out of the sample. The SiH content of the films on the other hand does not seem to exhibit any consistent behavior under the processing conditions used in these measurements. It is clearly not the source of the additional H needed to convert OH into H_2O, since the density is not nearly high enough, nor is the SiH concentration decreased when H_2O is produced.

The electrical charge trapping measurements were made using the avalanche injection technique[13] to introduce an electron current, with the trapped charge monitored with a capacitance measurement. The measurement, automatic data acquisition, and analysis techniques have been described elsewhere.[4] The samples used for these measurements were 1000 Å thick SiO_2 films thermally grown on Si wafers. Aluminum electrodes were deposited on the oxides to form an MOS structure. These samples were prepared similarly to the samples used for the infrared measurements but are necessarily different samples. It was not possible to make the electrical measurements on

oxides as thick as were necessary for the infrared measurements. Thick oxides or equivalently large trap concentrations are necessary for the relatively insensitive infrared technique, but the same large numbers of traps cannot be studied in the electrical measurements because the electric field from the trapped charge becomes too large for accurate measurement. It was also found to be impossible to make the infrared measurements on samples with an Al electrode present because the metal is too absorbing. These differences lead only to minimal uncertainty in the final results of the experiments.

The MOS samples were given the same types of processing treatments that the infrared samples were given. The results of these measurements are summarized in Table 2. The densities of the analyzed traps are given for each trapping cross section observed. The measurements directly give the interface trap density which has been converted in the table to a volume density assuming a uniform bulk trap distribution.[4] It is clear from these results that diffusion of H_2O into the samples produces an electron trap with a cross section of 1×10^{-17} cm.[2] Upon annealing in forming gas the density of this trap is drastically reduced and the density of the trap with a cross section of 2×10^{-18} cm^2 is increased. The 2×10^{-18} cm^2 trap cannot be detected in the H_2O diffused sample until after the annealing treatment. Unfortunately, the sensitivity to a low cross section trap in the presense of a higher cross section trap is very low. This leads to a large uncertainty in the possible density of

this trap in the H_2O diffused sample. Other measurements have shown[5] that an N_2 anneal behaves the same way as the F. G. anneal.

Comparison of the charge trapping results with the infrared absorption results shows that the trap with a cross section of 1×10^{-17} cm^2 is to be associated with SiOH groups in the SiO_2, and that the trap with a cross section of 2×10^{-18} cm^2 is to be associated with H_2O. The particular facts which lead to these correlations are: 1. the one to one correspondence between the concentrations of SiOH and the 1×10^{-17} cm^2 trap; and 2. the increase in both the H_2O concentration and 2×10^{-18} cm^2 trap density following a combination of H_2O diffusion and low temperature anneal. The actual densities measured by the two techniques cannot be compared directly since the oxide thicknesses, H_2O diffusion parameters and the presence of an Al electrode make the samples different. However, from the conditions, higher H_2O diffusion temperature and longer time, we would expect that the samples used for the infrared measurements would show somewhat higher densities of impurities, as observed.

From the details of the infrared results, we speculate on some of the dynamics of the trap formation. From the measurements we know that diffusing H_2O into SiO_2 results in the formation of SiOH groups. We further know that annealing the samples with or without an additional source of H_2 results in the conversion of SiOH to H_2O. This suggests that when the H_2O diffuses into the SiO_2 it finds a weak bond site and breaks an Si-O bond of

the Si-O-Si network. The H_2O also separates and forms two SiOH groups at adjacent sites. This mechanism would account for all of the atoms present and also account for the relative ease of annealing out the SiOH. In the annealing process the two SiOH groups would reform an H_2O and the original Si-O bond, and in addition the weak bond could be strengthened by a local rearrangement of the atoms. This latter point is supported by the difficulty in forming SiOH groups in the SiO_2 by drifting H_2O subsequent to a first drift and anneal. Further evidence for the double SiOH cluster is the frequency of the SiOH absorption. It is observed to be shifted from the normal SiOH vibrational frequency, and it has been speculated that the shift is due to hydrogen bonding in the sample.[7]

In summary we have made both infrared absorption measurements and charge trapping measurements on water diffused SiO_2 samples. We find that SiOH and H_2O are both present in the samples and that they each give rise to an electron trap in the oxide. The trapping cross section of each of these traps has been determined.

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TABLE 1

IMPURITY CONCENTRATION (cm^{-3})

Sample 1	SiH	SiOH	H_2O
Dry SiO_2	6.0×10^{15}	$< 5 \times 10^{17}$	1.3×10^{18}
H_2O Diffused (300 C, 10 min.)	5.4×10^{15}	1.5×10^{18}	1.1×10^{18}
H_2O Diffused (300 C, 20 min.)	1.2×10^{16}	1.2×10^{19}	1.1×10^{18}
F. G. Anneal (300 C, 30 min.)	1.3×10^{16}	8.0×10^{18}	1.8×10^{18}
F. G. Anneal (400 C, 30 min.)	1.4×10^{16}	1.5×10^{18}	2.9×10^{18}
N_2 Anneal (1000 C, 17 hrs.)	1.2×10^{16}	$< 5 \times 10^{17}$	1.4×10^{18}
Sample 2			
Dry SiO_2	1.6×10^{16}	8×10^{18}	1.8×10^{17}
H_2O Diffused (300 C, 30 min.)	5.2×10^{15}	2.2×10^{19}	5.1×10^{17}
N_2 Anneal (400 C, 30 min.)	1.1×10^{16}	$< 5 \times 10^{17}$	2.3×10^{18}

Table 1 shows the impurity concentration of various species determined from the infrared absorption analysis. Sample 1 was 3400 Å thick and grown in an ultradry environment. Sample 2 was 2000 Å thick and grown in a less carefully controlled dry environment. This may account for the somewhat different initial conditions of the oxides. The sequential processing steps that the samples underwent and the resulting changes in the impurity concentrations are shown.

TABLE 2

TRAP CONCENTRATION (cm^{-3})

	Trap Cross Sections	
Sample	1×10^{-17} cm^2	2×10^{-18} cm^2
Dry SiO_2	1.5×10^{16}	5×10^{16}
H_2O Diffused (250 C, 10 min.)	1×10^{18}	$< 1 \times 10^{17}$
Forming Gas Anneal (400 C, 30 min.)	3×10^{15}	1.5×10^{17}

Table 2 shows the trap concentrations for the two water related trapping cross sections observed in electrical measurements. The samples were 1000 Å thick and grown in an ultradry environment. The concentrations are shown for an as grown sample, for a sample which was water diffused, and for a sample which was both water diffused and forming gas annealed.

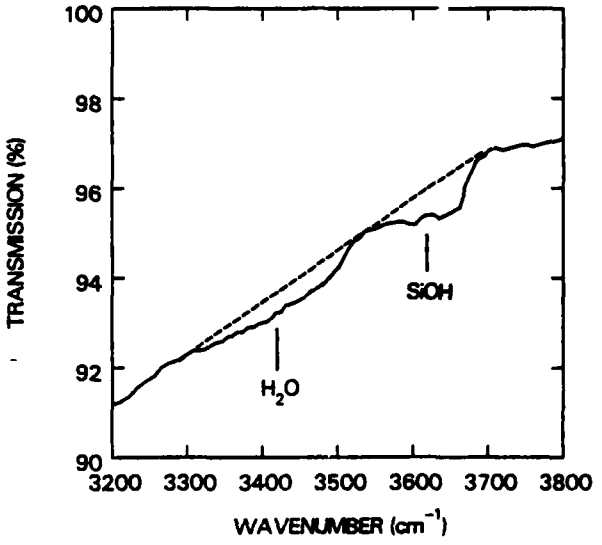

Figure 1 shows the transmission of the silicon total internal reflection element with a 3400 Å thick SiO_2 layer following a H_2O diffusion step. The absorption of the SiOH and H_2O vibrational modes in the SiO_2 sample is clearly evident. The dashed curve is the transmission without the vibrational modes present. Note that the transmission scale is highly expanded.

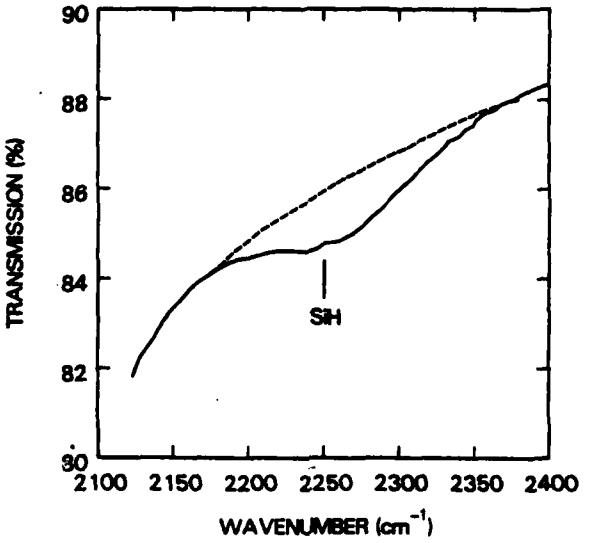

Figure 2 shows the transmission of the silicon total internal reflection element with a 3400 Å SiO_2 layer in a different frequency region. The absorption of the SiH vibrational mode in the SiO_2 sample is clear. The dashed curve in the transmission without the vibrational mode present.

Dual-Electron-Injector-Structure Electrically-Alterable Read-Only-Memory Modeling Studies

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ABSTRACT

Abstract: The threshold voltage shift of various dual electron injector structures which are composed of chemically-vapor-deposited stacks of Si-rich SiO_2, SiO_2, and Si-rich SiO_2 incorporated into floating polycrystalline-silicon-gate electrically-alterable read-only-memories has been studied as a function of write/erase voltages, write/erase times, and the initial charge state of the floating poly-Si gate and compared to a simple physical model for a variety of different device structures. This model depends on the interface limited (Si-rich SiO_2 - SiO_2 interfaces) enhanced current injection observed for the dual electron injector stacks at moderate gate voltages for both voltage polarities, the changing electric fields in the SiO_2 layers as the floating polycrystalline silicon gate electrode is charged or discharged, and the voltage dependent capacitance of the dual electron injector stack. Good agreement is observed between the experimental data and this model. This model will be the starting point in designing more complicated device arrays for non-volatile memory applications.

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I. Introduction

Several recent publications have shown that chemically-vapor-deposited (CVD) Si-rich-SiO_2 – SiO_2 – Si-rich-SiO_2 stacks can be used in floating polycrystalline-Si (poly-Si) electrically-alterable read-only-memories (EAROMs) as a means for putting electrons on or removing them from the floating poly-Si charge storage layer [1-3]. This CVD stack is called a dual electron injector structure (DEIS) since it will give enhanced electron injection for either polarity. The device is shown schematically in Fig. 1, and it is called a DEIS EAROM. This article will be concerned with developing a simple physical model which can predict accurately the threshold voltage shift after a write/erase operation for any type of DEIS EAROM. This model is necessary for predicting the operation and aiding in the development of more complicated EAROM circuits using the DEIS concept.

The enhanced electron injection phenomenon which occurs at moderate gate voltages from the contact at the lower potential is believed to be due to electric field distortion at the Si-rich-SiO_2 – SiO_2 interface [4,5]. This electric field distortion is caused by the two phase nature of Si-rich SiO_2 [6-8] where Si islands $\lesssim$ 50 Å in size are surrounded by SiO_2 for the 46% atomic Si materials used in this study. At moderate gate voltages, electrons move easily from the contact (poly-Si or Al) through the Si-rich SiO_2 region (probably by direct tunneling or percolation between Si islands for Si-rich SiO_2 material with $\gtrsim$ 46% atomic Si [4]) to the Si-rich SiO_2 interface with the SiO_2 layer. Here electrons on the last layer of Si islands are injected into the SiO_2 by field-enhanced Fowler-Nordheim tunneling with the electric field enhancement due to the finite curvature of the Si islands [9]. DEISs show an electrical asymmetry in the injected current when deposited on Si (either smooth single crystal Si or rough poly-Si) with an Al or poly-Si top gate electrode [1-3]. This asymmetry where the bottom Si-rich SiO_2 layer injects at lower gate voltages than the top Si-rich SiO_2 layer is believed to be due to microscopic differences in the two Si-rich SiO_2 interfaces since the bottom injector is deposited on Si and the top injector on SiO_2 [2,3].

At lower gate voltages, the electrons can not move as readily through the Si-rich SiO_2 layer because of the highly non-ohmic character of the Si-rich SiO_2 layer [7] and the reversible space charge this layer builds up [4]. This property leads to the outstanding retention of the electrons stored on the floating poly-Si layer and the decrease in the number of low voltage breakdown events observed [2,3].

DEIS EAROMs can be written or erased > 10^4 times (electrons are put on or taken off the floating poly-Si storage layer) at much lower voltages and in shorter times than

commercially available metal-silicon nitride-silicon dioxide-silicon (MNOS) [10,11] or floating-gate avalanche-injection metal-oxide-semiconductor (FAMOS) devices [11,12]. A recent publication by these authors demonstrated writing or erasing in 5 msec at $\lesssim$ 16 V and in 2 μsec at $\lesssim$ 23 V with excellent charge retention using a coupling coefficient (defined as the ratio of the voltage drop across the DEIS stack to the total applied voltage) of 0.5 [2]. Increasing the coupling coefficient to $\gtrsim$ 0.9 will decrease these write/erase voltages further by about a factor of two.

The ultimate cycling limit of DEIS EAROMs before threshold voltage window collapse has been demonstrated to be due to electron trapping in the intervening CVD SiO_2 [3]. This limit can be from 10^4 to 10^6 write/erase cycles depending on the amount of high temperature annealing done to minimize the trapping sites which are related to H_2O [13]. This limit is similar to most non-volatile memories using SiO_2 layers, although some MNOS structures have been reported to cycle 10^{10} times before threshold voltage window collapse [14].

The DEIS EAROM is also inherently a better structure from the point of view that it writes or erases at lower fields by about a factor of two and it will suffer less from low voltage breakdown events than any of the new EAROM devices. These new devices are written or erased using Fowler-Nordheim tunneling into only SiO_2 from planar interfaces for the injection mechanism to put on or take off electrons from a floating poly-Si storage layer [15,16]. Another new device that uses field-enhanced Fowler-Nordheim tunneling into SiO_2 from the rough top surface of deposited poly-Si films also writes/erases at higher voltages and requires three layers of poly-Si [17].

This article will show that all write/erase operations of DEIS EAROMs can be explained using a simple physical model which depends on the interface-limited (Si-rich-SiO_2 – SiO_2 interfaces) enhanced current injection observed for DEIS stacks at moderate gate voltages for both voltage polarities [1-5], the changing electric fields in the SiO_2 layers as the floating poly-Si gate electrode charges or discharges during the write and erase operations [3], and the voltage dependent capacitance of the DEIS stack [3-5]. Calculations using this simple model which will be discussed in detail in section II will be shown to give good agreement in section III with a variety of experimental measurements of the threshold voltage shift ΔV_T on different types of DEIS EAROMs after writing or erasing where the write/erase times, voltages, and initial charge state of the floating poly-Si storage layer have been varied.

II. DEIS EAROM Model

The model describing the DEIS EAROM operation during writing or erasing is based on the behavior of the injected electronic particle current at the Si-rich-SiO_2 – SiO_2 interfaces as the floating poly-Si gate charges or discharges, respectively. The Si-rich SiO_2 layers are much less resistive than the intervening SiO_2 [4,5,7] and therefore the current injection mechanism is controlled by the Si-rich-SiO_2 – SiO_2 interfaces [1-5]. Also, the voltage drop across the Si-rich SiO_2 layers is small and therefore, neglected in the modeling, as compared to that dropped across the intervening CVD SiO_2 and the thermally grown SiO_2 layer between the Si substrate and the floating poly-Si layer. For the write operation, the oxide electric field near the top Si-rich-SiO_2 – SiO_2 interface will decrease as the floating poly-Si storage layer fills with electrons. This write operation from an uncharged initial state of the floating poly-Si layer is depicted schematically in Fig. 2a in terms of energy band diagrams. Similarly, the oxide electric field near the bottom Si-rich-SiO_2 – SiO_2 interface will decrease as electrons are removed during an erase operation from the floating poly-Si layer. The erase operation from an uncharged initial state of the floating poly-Si layer is depicted schematically in Fig. 2b in terms of energy band diagrams. As electrons are removed during the erase operation, ionized donors (which are positively charged) are left behind.

The areal electronic particle current density (defined as $J_p = I_p/A_1$ where I_p is the electronic particle current and A_1 is the injecting area of the device) as a function of the intervening CVD SiO_2 electric field (defined as $\mathcal{E}_1 = V_1/\ell_{o_1}$ where V_1 is the voltage drop across the intervening CVD oxide layer of the DEIS stack neglecting the voltage drops across the Si-rich SiO_2 layers and ℓ_{o_1} is the thickness of the CVD SiO_2 layer) is shown in Fig. 3 for numerous large area (.006 cm^2) capacitor structures and DEIS EAROMs [3]. This current has been demonstrated to be consistent with a mechanism controlled by field-enhanced Fowler-Nordheim tunneling from the last layer of Si islands in the Si-rich SiO_2 layer into the SiO_2 layer at the Si-rich-SiO_2 – SiO_2 interface [4,5]. The temperature dependence of these injected currents from 77°K to 500°K has also been shown to be consistent with Fowler-Nordheim tunneling [4].

The assumption that J_p can be represented by a uniform current per unit electrode area even though the actual carrier injection mechanisms are believed to be localized at the injecting interfaces has been justified in previous publications for larger area (.006 cm^2) capacitor structures using single [5] and dual [1] Si-rich SiO_2 injectors. The reasoning is that the Si islands in the Si-rich SiO_2 layers which inject carriers are very small ($\leq$ 50 Å) and

densely packed for 46% atomic Si materials compared to the dimensions of the control and floating gate electrodes which are on the scale of microns ($\gtrsim 10^4$ Å).

The techniques for measuring particle current densities on field-effect-transistor (FET) [3] or capacitor [4] structures have been described in detail elsewhere. With capacitors, the currents flowing in a DEIS stack sandwiched between Si and Al contacts are measured directly [4]. With FETs, the currents flowing in DEIS stacks sandwiched between control and floating poly-Si electrodes of an EAROM are measured indirectly using charge build-up on the floating poly-Si and the subsequent threshold voltage shift it produces as a self integrating detector for current flow [3]. The FET currents and electric fields are therefore time averaged values [3].

Clearly from Fig. 3, the current density as a function of the electric field can be approximated over the range of interest used here by the simple relationship

$$J_p = J_p^i \exp\left[S(\mathcal{E}_1 - \mathcal{E}_1^i)\right] \tag{1}$$

where the superscript i refers to a reference level and S is the slope of the appropriate curve for either writing or erasing. Equation 1 is a reasonable phenomenological approximation to the more complicated Fowler-Nordheim relationship over the range of interest here and it will be shown to give good agreement with the actual experimental threshold voltage shift, ΔV_T, data in section III-B. The electric field $\mathcal{E}_1(t)$ at any time t which changes as electrons build-up on or are taken off the floating poly-Si layer is given by the relationship [5,18]

$$\mathcal{E}_1(t) = \frac{V_g - \Phi_{ms} - \Psi_s}{\ell_o} - \left(1 - \frac{\ell_{o_1}}{\ell_o}\right)\frac{Q(t)}{A_1 \varepsilon_o} \tag{2}$$

where V_g is the control gate voltage applied during writing or erasing ($V_g = V_w$ or V_E, respectively), $\Phi_{ms} \approx -.9$ V is the work function difference between the control gate (which is degenerate n-type poly-Si) and the Si substrate (which is 0.5 Ωcm p-type single crystal Si), Ψ_s is the silicon substrate surface potential, $\ell_o = \ell_{o_1} + \ell_{o_2}$ is the total SiO_2 thickness including the intervening CVD SiO_2 layer of thickness ℓ_{o_1} and the thermal gate oxide of thickness ℓ_{o_2} between the Si substrate and the floating degenerate n-type poly-Si layer, ε_o is the low-frequency permittivity of SiO_2 which is equal to 3.9 × (permittivity of free space = 8.86 × 10^{-14} F/cm), and Q(t) is the total charge (either negative for electrons or positive for ionized donors) on the floating poly-Si layer which also has an area A_1 equivalent to that of the control gate for the devices studied here. Substituting equation 2 into equation 1, taking the derivative with respect to time, substituting the relationship $I_p(t) = dQ(t)/dt$, and finally

integrating both sides of the resulting equation from the start of the write or erase pulse at t=0 to any time, t, yields

$$\frac{J_p(t)}{J_p(0)} = \frac{1}{\frac{J_p(0)\, S\, t\, A_1}{\ell_{o_1} C_T} + 1} \tag{3}$$

where $C_T = C_1 + C_2 = \varepsilon_o A_1 (1/\ell_{o_1} + 1/\ell_{o_2})$ is the sum of the relevant capacitances of the device as shown in Fig. 4a. Using equation 1, it can easily be shown that

$$\Delta \mathscr{E}_1(t) = \mathscr{E}_1(t) - \mathscr{E}_1(0) = \frac{\ln\left[\frac{J_p(t)}{J_p(0)}\right]}{S}. \tag{4}$$

The change in the threshold voltage shift Δ (ΔV_T) where $\Delta V_T = V_T(t) - V_{T_i}$ (V_{T_i} is the threshold voltage of an as-fabricated structure with the floating gate in an uncharged state) which is the measurable quantity of interest in the experiments that are described in section III-B is defined as [3,19]

$$\Delta(\Delta V_T) = \Delta V_T(t) - \Delta V_T(0) = \frac{+\ell_{o_1} C_T\, \Delta \mathscr{E}_1}{C_1^*} = -\frac{\Delta Q}{C_1^*} \tag{5}$$

where ΔQ is the charge added or removed from the poly-Si floating gate during writing or erasing and $C_1^* = A_1 (\ell_{o_1}/\varepsilon_o + \ell_n/\varepsilon_n)^{-1}$ is the <u>low field</u> (the threshold voltage of the devices is determined at applied control gate voltages which are much smaller than write/erase voltages) capacitance of the DEIS stack which must include the series contribution of both Si-rich SiO_2 injectors which have a low-field, low-frequency permittivity of $\varepsilon_n \approx 7.5 \times$ (permittivity of free space) [4] and a total sum of thicknesses ℓ_n. For write/erase operations at higher voltages, ε_n effectively becomes very large [4] due to the increase in conductivity of the Si-rich SiO_2 layers with respect to the intervening CVD SiO_2 layer [4,7]. Therefore, the high-field capacitance of the DEIS stack C_1 is $\approx A_1 \varepsilon_o / \ell_{o_1}$ [4,5] and the Si-rich SiO_2 layers can be ignored. For devices with Si-rich SiO_2 layers with a much larger Si content than used here (> 46% atomic Si), the low-field, low-frequency permittivity of the Si-rich SiO_2 should become larger due to its increased conductivity and cause $C_1^* \rightarrow C_1$. Also, if the floating gate is sufficiently overcharged, the electric field across the DEIS stack might become large enough to force $C_1^* \rightarrow C_1$ even at the low applied gate voltages used for determining V_T because of the internal electric field generated by the charge on the floating gate itself. For writing or erasing from an initially uncharged floating gate condition, $\Delta(\Delta V_T) \rightarrow \Delta V_T$ and $\Delta Q \rightarrow Q$. The

series of equations 1-5 determine the value of $\Delta(\Delta V_T)$ using $J - \mathcal{E}_1$ data as shown in Fig. 3 to determine S, J^i, and $\mathcal{E}_1^i$ for either writing or erasing. The computer simulations which are compared to experimental data in section III-B are based on these equations and Fig. 3.

Equations 1 and 3-5 are general equations not only for the equal area three port structures used in this study as depicted in Fig. 4a, but also for any of the devices depicted in Fig. 4. These other devices are three port structures with unequal floating and control gate areas (Fig. 4b) and four port structures (Fig. 4c). The smaller area of the gate with the DEIS stack under it forces a larger fraction of the applied voltage across the DEIS as compared to the equal area 3 port structure in Fig. 4a. This results in lower applied voltages for write and erase operations. Using equation 5 and capacitive coupling considerations, equation 2 can be generalized to

$$\mathcal{E}_1(t) = \frac{\chi(V_g - \Phi_{ms} - \Psi_s)}{\ell_{o_1} C_T} + \frac{C_1^* \Delta V_T(t)}{\ell_{o_1} C_T} \qquad (6)$$

for any of the types of structures depicted in Fig. 4. Table I summarizes the values of χ and C_T used in equations 3, 5, and 6 for write and erase operations. In this table, the gate to which the voltage V_g is applied during writing or erasing is indicated by the appropriate capacitance of that gate. Also the sign of the applied voltage is indicated by a superscript (V_g^+ and V_g^- for positive and negative applied voltage bias, respectively).

If the gate used during reading the four port device (that is, determining the threshold voltage which involves measuring the drain current as a function of the gate voltage [19]) in Fig. 4c is the gate with capacitance C_3, then C_1^* should be replaced by C_3 in equations 5 and 6. During reading the four port structure in Fig. 4c, the opposite gate (with either capacitance C_3 or C_1^*) not used in reading, is grounded. If both gates with capacitances C_1^* and C_3 in the four port structure are biased to the same voltage during reading, then C_1^* should be replaced by $C_1^* + C_3$.

III. Experimental

A. Device Fabrication and Measurement Techniques

The enclosed FET structures used here were fabricated using a self-aligned, double poly-Si process which gave equal control and floating poly-Si gate areas. The two types of devices used in this study (#7 and #8) had channel lengths of either 2.54×10^{-4} cm or 3.18×10^{-4} cm after photolithography, but effectively either $\approx 1.8 \times 10^{-4}$ cm or

$\approx 2.4 \times 10^{-4}$ cm after diffusion drive-in and subsequent high temperature processing, respectively. The channel width was 1.62×10^{-2} cm and the FET channel area was effectively either 2.9×10^{-6} cm^2 for #7 or 3.9×10^{-6} cm^2 for #8. The actual injecting area for writing and erasing was 8.4×10^{-6} cm^2 for #7 or 9.4×10^{-6} cm^2 for #8 due to capacitive considerations. These differences in area for devices #7 and #8 had no effect on the experiments studied here. After defining thick field oxide regions, the devices were fabricated by thermally oxidizing 0.5 Ωcm <100> p-type single crystal silicon substrates to an SiO_2 thickness of either 290 Å or 100 Å for the different device runs which are called MDT-DIS 2 and MDT-DIS 3, respectively. Next a 3,500 Å thick poly-Si layer was deposited and doped n-degenerate with $POCl_3$ (this will form the floating charge storage layer) followed by the injector stack consisting of CVD deposited SiO_2 and Si-rich SiO_2 layers as listed below from bottom to top for the various device runs:

MDT-DIS 2-A,B 150 Å Si-rich-SiO_2 – 150 Å SiO_2 –. 150 Å Si-rich-SiO_2

MDT-DIS 3-A,B 100 Å Si-rich-SiO_2 – 100 Å SiO_2 – 100 Å Si-rich-SiO_2

A top 3500 Å thick poly-Si n-degenerate layer, similar to the first poly-Si layer, was then deposited and doped. Next, the gate stack was etched with plasma etching, reactive ion etching (RIE), and wet etching to define the source and drain. The source and drain were diffused, a 1000 Å oxide was regrown at 1000°C over the source and drain, and a protective 3000 Å layer of CVD SiO_2 followed by a phosphosilicate glass (PSG) passivation layer were deposited and annealed at 1000°C. Finally, contact holes to the source, drain and top poly-Si gate were defined and etched, followed by Pd_2Si and Al metallizations and a 400°C anneal for 20 minutes in forming gas (90% N_2 - 10% H_2). All CVD Si-rich SiO_2 layers contained 46% atomic Si and were deposited at 700°C using a ratio of concentrations of N_2O to SiH_4 in the gas phase, R_o, of 3 [4,7]. All CVD SiO_2 layers were deposited at 700°C using a concentration ratio of N_2O to SiH_4 in the gas phase of 100.

On the FET structures, the d.c. drain current as a function of gate voltage with 100 mV applied to the drain and with the source and substrate at ground potential was used to determine the transistor turn-on or threshold voltage, V_T. This in turn is a measure of the charge state of the floating poly-Si electrode (written, erased, or neutral). A low noise voltage ramp with adjustable ramp rates was used to supply the gate voltage and a Keithley model #610C electrometer was used to measure the electron current flowing from source to drain. This electrometer was operated with a 100 Ω resistance in series with the source to drain resistance. This 100 Ω resistor had less than 4% of the 100 mV applied to the drain dropped

across it for the measurements performed here. Hewlett-Packard pulse generators (model #214A) were used to supply the write and erase voltages to the gate electrode.

B. Experimental Results and Model Comparison

In this section, experimental data on the two sets of devices with equal control and floating poly-Si gate areas as described in section III-A will be compared to the computer simulation of the model described in Section II. The threshold voltage shift for the write and the erase operation of the DEIS EAROMs (MDT-DIS 2-A,B and MDT-DIS 3-A,B) was investigated as a function of write/erase voltages, times, and the initial charge state of the floating poly-Si charge storage layer.

Figure 5 shows the exponential approximation to the data shown in Fig. 3 used in all simulations discussed in this section. From the data of Fig. 5, the values of J_p^i, $\mathcal{E}_1^i$, and S used in equation 1 can be deduced. These values are $S = \pm 4 \times 10^{-6}$ cm/V, $J_p^i = \pm 10^{-5}$ A/cm^2, $\mathcal{E}_1^i = +4 \times 10^6$ V/cm and $\mathcal{E}_1^i = -5.4 \times 10^6$ V/cm for erasing and writing, respectively, where the sign convention used is for the positive direction defined from the control gate towards the Si substrate [5,18]. Figure 6 shows the magnitude of ΔV_T as a function of the magnitude of $V_{W/E}$ for writing and erasing from an uncharged virgin state of the EAROM. The comparison between the experimental data points and the results computed from the model are good.

Figures 7 and 8 show a comparison with the predictions of the model and the experimental data on MDT-DIS 2-B for the threshold voltage shift as a function of the write or erase pulse duration, respectively, for several constant write/erase gate voltage amplitudes. For all cases in Figs. 7 and 8, writing or erasing is done from the uncharged virgin state of the EAROM FET. Figures 9 and 10 compare the threshold voltage shift as a function of write or erase pulse duration, respectively, under a constant gate voltage amplitude for DEIS EAROMs from the MDT-DIS 2-B wafer for an uncharged floating gate condition and a floating gate charged initially to a threshold voltage shift of -6.3 V before writing (Fig. 9) or of $+4.7$ V before erasing (Fig. 10). As seen in Figs. 7-10, the experimental data and the model predictions are in good agreement.

IV. Conclusions

A simple phenomenological model based on experimental current-field characteristics has been used to predict DEIS EAROM operation under a variety of conditions with a variety

of devices. This model easily shows the physics behind the device operation, and it is needed in predicting the operation of more complicated DEIS EAROM arrays. The phenomenological current-field relationship used (equation 1) allows a rather simple mathematical solution for ΔV_T, and it clearly shows the salient features expected if a more rigorous Fowler-Nordheim relationship was used instead.

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TABLE I

Device	Condition	C_T	χ
3 port/equal area	write: C_1 at V_g^- erase: C_1 at V_g^+	$C_1 + C_2$	C_2
3 port/unequal area	write: C_1 at V_g^- erase: C_1 at V_g^+	$C_1 + C_2$	C_2
4 port	write: C_1 at 0 V C_3 at V_g^+	$C_1 + C_2 + C_3$	$-C_3$
4 port	erase: C_1 at V_g^+ C_3 at 0 V	$C_1 + C_2 + C_3$	$C_2 + C_3$

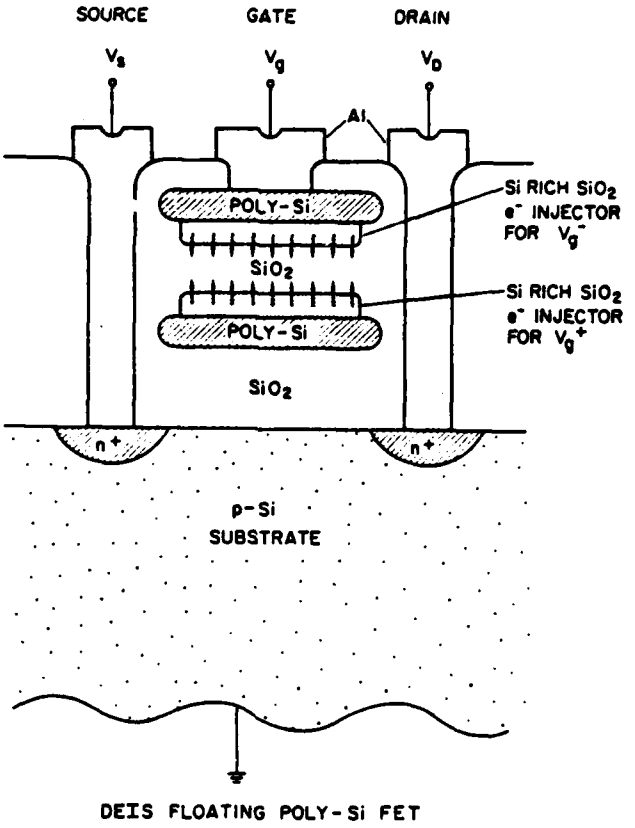

Figure 1. Schematic representation of a non-volatile n-channel field effect transistor memory using a dual electron injector stack between a control gate and a floating poly-Si layer. Writing (erasing) is performed by applying a negative (positive) voltage, to the control gate which injects electrons from the top (bottom) Si-rich SiO_2 injector to the floating poly-Si storage layer (back to the control gate). Structure is not drawn to scale.

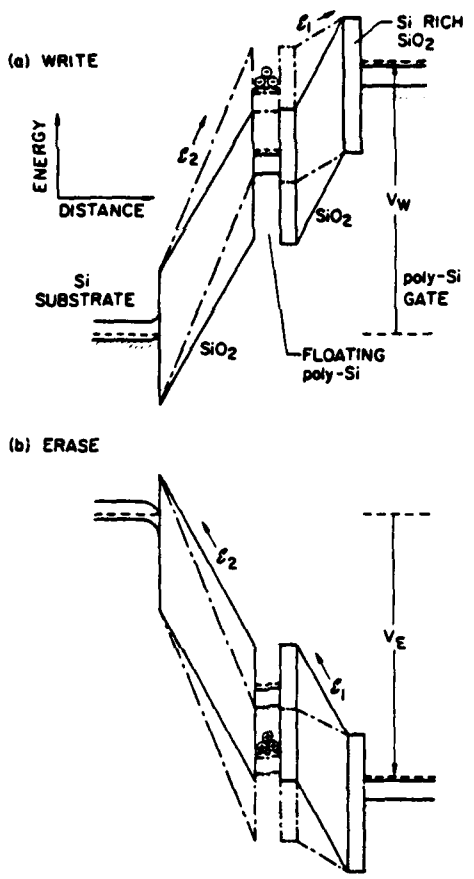

Figure 2. Schematic energy band representation of an FET using Si-rich SiO_2 injectors for (a) writing and (b) erasing a floating poly-Si charge storage layer. Solid and dot-dash lines represent the uncharged and charged [either (a) negatively or (b) positively] EAROM, respectively. $\mathcal{E}_1$ and $\mathcal{E}_2$ indicate the average electric fields in the CVD and thermal SiO_2 layers, respectively.

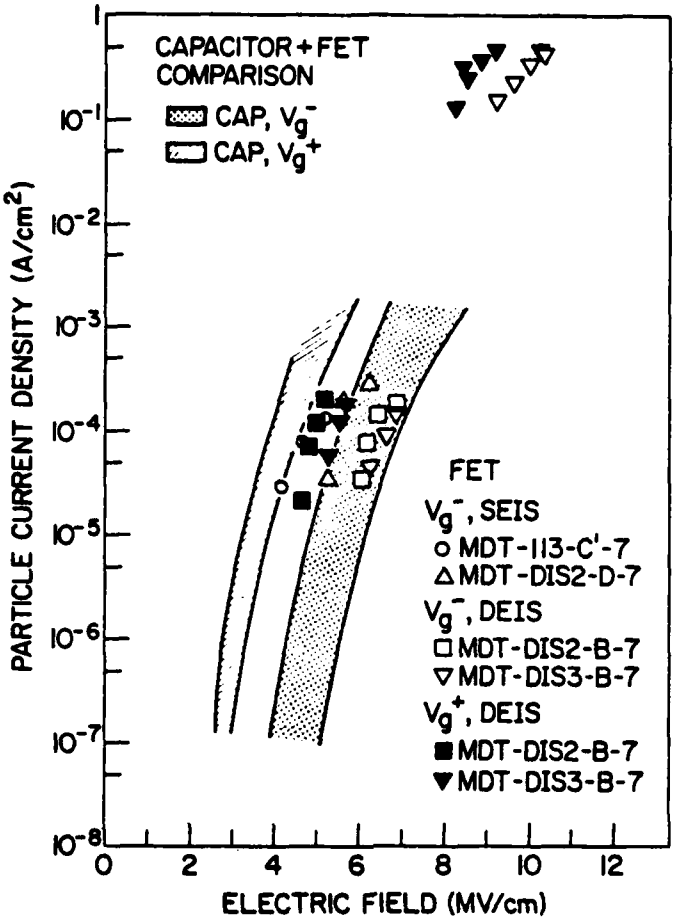

Figure 3. Comparison of the electronic particle current density as a function of the electric field for the oxide layer in DEIS and SEIS stacks incorporated into large area capacitors with smooth single crystal Si and Al contacts and small area EAROM FETs with poly-crystalline Si electrodes. Taken from reference 3.

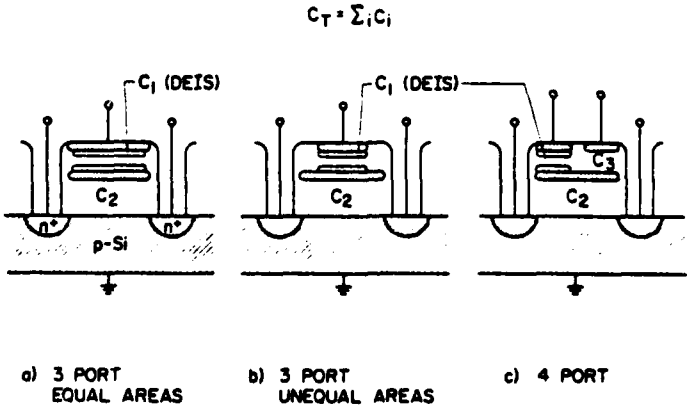

Figure 4. Schematic illustration of different types of DEIS EAROM structures whose operation can be simulated by the model discussed in the text.

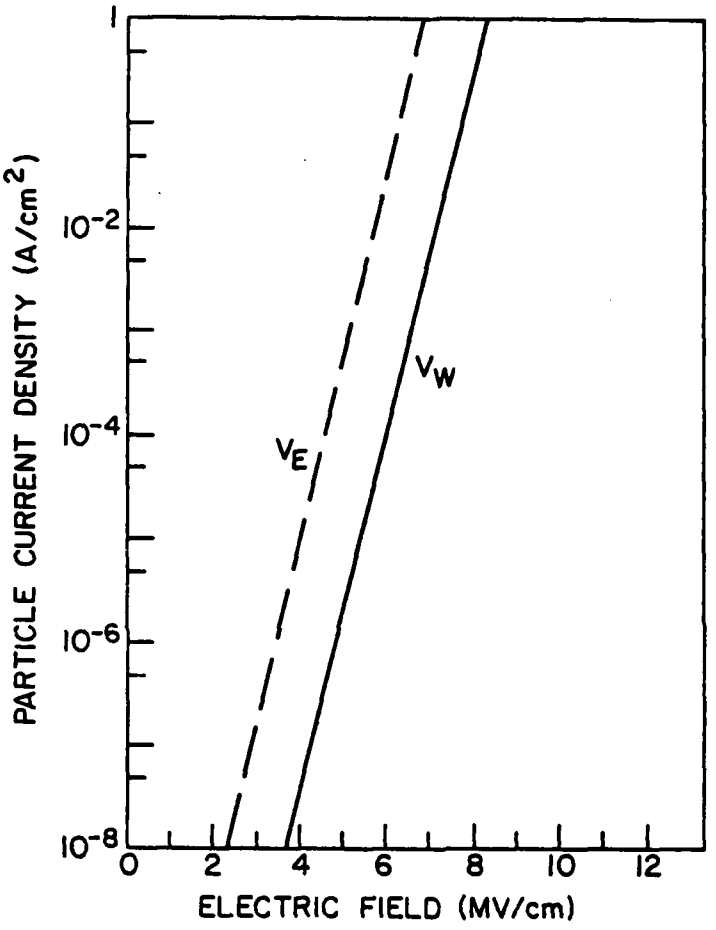

Figure 5. Exponential approximation to the data shown in Fig. 3 used in the model simulations discussed in section II for writing or erasing a DEIS EAROM.

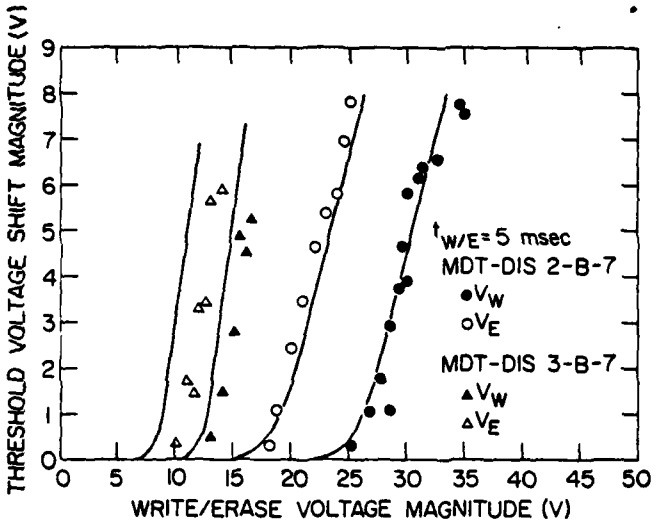

Figure 6. Magnitude of the threshold voltage shift as a function of the magnitude of the write or erase gate voltage for different types of three port EAROMs with control and floating poly-Si gates with identical areas. All devices were written or erased from an as-fabricated uncharged floating poly-Si gate condition using a pulse duration of 5 msec. Solid lines are simulations from the model discussed in section II using the approximations of Fig. 5, while solid or open symbols are experimental data.

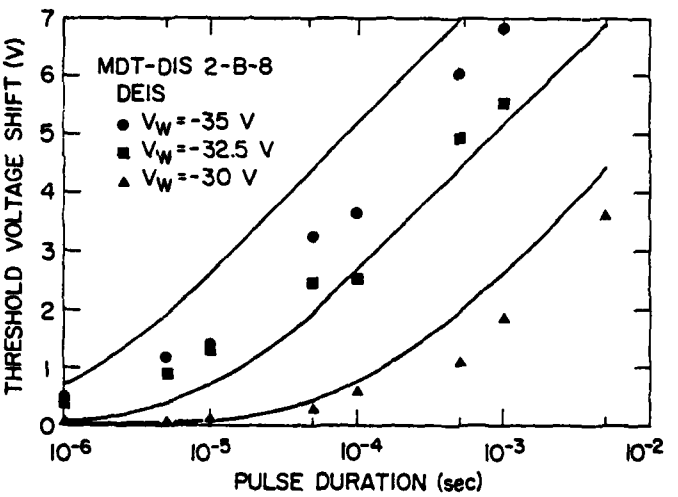

Figure 7. Threshold voltage shift as a function of write pulse duration on devices from the MDT-DIS 2-B wafer for various gate voltage V_W conditions. All devices were written from an as-fabricated uncharged floating poly-Si gate condition. Solid lines and solid symbols have the same meaning as in Fig. 6.

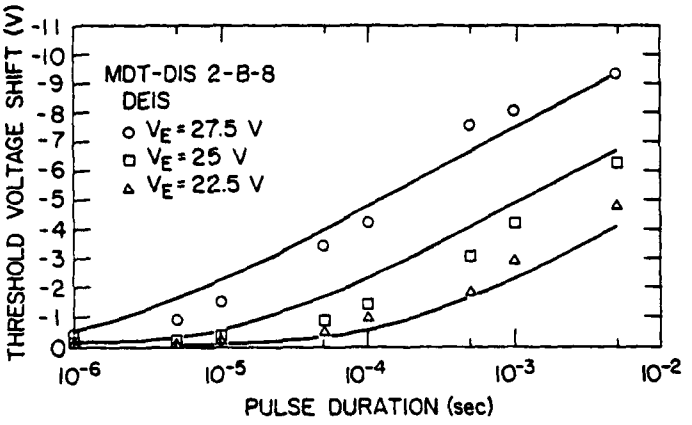

Figure 8. Threshold voltage shift as a function of erase pulse duration on devices from the MDT-DIS 2-B wafer for various gate V_E conditions. All devices were erased from an as-fabricated uncharged floating poly-Si gate condition. Solid lines and open symbols have the same meaning as in Fig. 6.

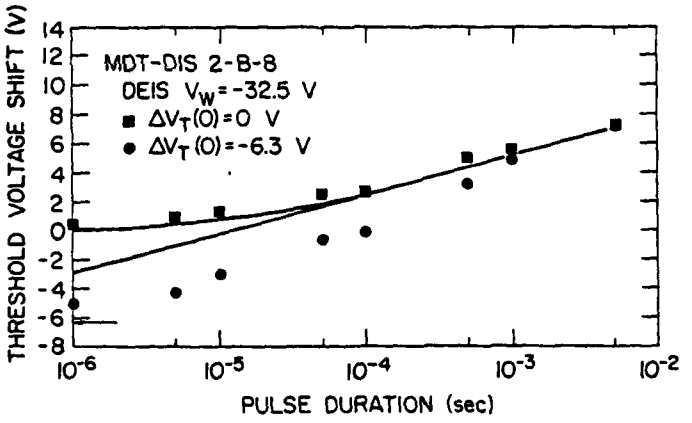

Figure 9. Comparison of the threshold voltage shift as a function of pulse duration for writing from either an as-fabricated uncharged state or a positive charge state (erased state) of the floating poly-Si gate on devices from the MDT-DIS 2-B wafer. Solid lines and solid symbols have the same meaning as in Fig. 6. The negative threshold voltage shift of the initial positive charge state of the floating gate, which was set by erasing an as-fabricated uncharged device, is indicated by the arrow.

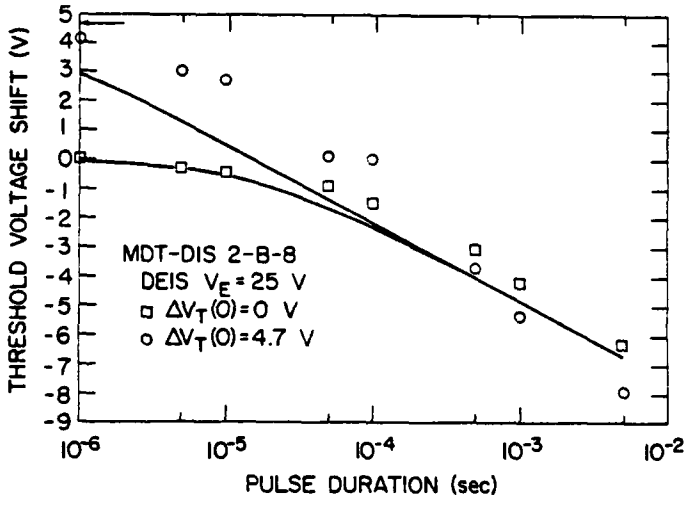

Figure 10. Comparison of the threshold voltage shift as a function of pulse duration for erasing from either an as-fabricated uncharged state or a negative charge state (written state) of the floating poly-Si gate on devices from the MDT-DIS 2-B wafer. Solid lines and open symbols have the same meaning as in Fig. 6. The positive threshold voltage shift of the initial negative charge state of the floating gate, which was set by writing an as-fabricated uncharged device, is indicated by the arrow.

VERY THIN GATE INSULATORS

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ABSTRACT

Very thin gate insulators (5 to 20 nm) are very important in electrically alterable read only memories (EAROMs) and future VLSI circuits. The major problem in silicon dioxide is yield and reliability. The reliability problem may be controlled by the use of trapping. Such oxides also show increased resistance to radiation damage and with reduction of bulk effects, interface effects become important. Thermally grown silicon oxynitride films may be used as a substitute for oxide films.

I. Introduction

With the rapid advances in silicon integrated circuit technology, very thin gate insulators (5 to 20 nm) are becoming very important as key elements in basic circuit devices. There are two places where high quality gate insulators are essential to proper device operations. The first is the gate insulator in MISFETs for VLSI circuits. As the lateral dimensions in VLSI circuits are reduced to increase density, the vertical dimensions, including the gate insulator thickness, have to be reduced to maintain proper FET functions. It was projected that for 1 μm channel length MOSFETs, 20 nm oxides would be used for the gate (1). Experimental circuits with channel length close to 1 μm have already been demonstrated by using electron beam lithography (2). In a production environment, high quality 20 nm oxide will have to be prepared routinely. The yields must be high and it should not be degraded by subsequent processing. Long term reliability of the oxide is also important.

Increasingly, high quality gate insulators are being used in a new and very important device: electrically alterable read only memory (EAROMs) (3-8). In this application, the insulator is used as a "gate" to control the flow of electrons into and out of a floating polysilicon gate region. The conduction of the insulator is highly nonlinear. At low field, it is a very good insulator and there is no leakage of charge from the floating gate during normal read cycles. At high field (~ 10 MV/cm), carriers can flow through the insulator by Fowler-Nordheim tunneling (9). The prosess is very efficient with low power requirement because of the low current. However, for a conventional 100 nm oxide, a voltage of 100 volts is needed to give the desired field which is not practical in integrated circuits. The write and erase voltages required can be lowered by making use of enhanced injection from silicon rich silicon dioxide (3) or asperities on polysilicon surfaces (6), but it is inevitable that thinner oxides are used even when there is enhanced injection (3). Different workers have selected an oxide thickness of 20 nm for use in such circuits (4,5). The thickness probably represents a compromise between yield and

practical write and erase voltages. In fact, an EAROM structure with a 5 nm oxide was recently reported (7,8). Not only does it have low write and erase voltages, but also the write and erase time is only 50 nsec (8). Because of the very high field used in EAROMs, the quality of the insulator is even more important. It must be able to sustain high electric field repeatedly and be able to carry the current with little degradation in time due to trapping effects (3,4). In fact, this is one area where the property of the insulator can be engineered to give the optimal characteristics. Once the degradation problem due to electron trapping is solved and given the very high speed operation, it is possible to fabricate a non-volatile random access memory.

Silicon dioxide is probably one of the most studied insulators, but most of the work has been in thicker oxides of around 100 nm. For oxides thinner than 20 nm, most of the work was done on oxides of tunneling thickness (< 5 nm) (10). However, the oxides were usually prepared by special methods and the properties reported were only relevant to tunnel oxides. It is only recently that an attempt was made to link the properties of tunnel oxides to conventional thick oxides (11). Besides silicon dioxide, there has recently been a lot of interest in silicon oxynitride prepared by direct nitridation as an alternative gate insulator (12-15). The maximum thickness reported is 10 nm and it offers many advantages over silicon dioxide in this very thin region, as well as major disadvantages. It is the purpose of this paper to discuss some of the problems and advantages in the use of these very thin insulators.

II. Growth of Very Thin Silicon Dioxide

Conventional silicon dioxide films have usually been grown at 1000°C or above (16). Using an oxidant of either oxygen or steam at atmospheric pressure, high quality oxides can be prepared. This, however, is not practical for very thin oxides. Using similar growth conditions as thick oxides, growth time would be short, making control of thickness difficult. In order to overcome the problem, variations of the basic oxidizing conditions are used, mostly along two directions. The first is to use lower temperatures. Temperatures as low as 600°C were used for growth in steam (17) but usually, temperatures in the range of 800°C to 900°C were used (18-21). This is in fact conforming to the general trend in VLSI circuits with lower temperature processing. The second is to reduce the effective oxidant pressure, either by diluting oxygen (22,23) or water vapor (21) with an inert gas or by using a low pressure oxidation system (24). Under such conditions, temperatures above 1000°C can be used to give reproducible thickness oxides. Figure 1 shows typical growth curves in dry oxygen and nitrogen with 2000 ppm of water at three different temperatures.

The growth kinetics for oxidation in dry oxygen at atmospheric pressure can best be characterized by the linear-parabolic rate model (18-21). The rate constants are very sensitive to moisture content and trace amounts of water vapor increase the parabolic rate significantly to dominate the growth (21,25). For oxidation in 10^{-2} atm partial oxygen pressure (22) or low pressure oxygen (0.25 to 2.0 Torr) (24), the parabolic rate also dominates. For oxygen partial pressure less than 10^{-2} atm, it was reported that an inverse-logarithmic law gave the best fit to data (22). But questions were raised as to whether such a model was appropriate, and the data could also be fitted to a linear-parabolic model (24). The growth kinetics is also affected by the surface condition of the

wafer before start of oxidation (26). Different surface cleaning techniques give different initial growth rate. This may be due to the presence of a native oxide. For most reproducible results, the surface can be etched slightly by HCl before oxidation (27). It is important to realize that the growth of oxides in the very thin regime is more critical than thicker oxides.

For better results, it may even be necessary to use more complicated oxidation procedures. One example is a two-step oxidation method which was recently reported (28). In the process, oxidation is carried out at a lower temperature with HCl for control of growth rate. The oxide is then annealed at a higher temperature to activate the passivation effect of HCl (29). By controlling the temperature and oxidation environment, reproducible thickness oxides can be obtained. However, it is very important to evaluate the difference in electrical properties resulting from the different growth conditions. Processes like the two-step oxidation may be needed to give, as will be mentioned later, the best electrical characteristics of the silicon-silicon dioxide interface. It is important to optimize the processes to give high yield and the highest quality oxide.

III. Breakdown and Reliability

Electrical breakdown in silicon dioxides has been studied as a function of oxide thickness (30-32). It was shown that for intrinsic breakdown, the breakdown field was increased for decreasing oxide thickness, going from less than 10 MV/cm for oxides thicker than 50 nm to larger than 14 MV/cm for oxides thinner than 15 nm (Figure 2). This is one advantage of the very thin oxides. On the other hand, it has also been shown that the defect density increases with decreasing thickness, (24,32) giving a higher probability for low field breakdown in very thin oxides (Figure 3) This is one area that requires the most understanding and improvement. The question is whether the high defect density is intrinsic to very thin silicon dioxides or if it can be improved with further improvement in cleanliness and control of oxidation.

There is evidence that in the very thin regime (< 20 nm), there are definite relationships between the physical properties of the oxide and its electrical properties. High resolution transmission electron micrographs of oxides grown in dry oxygen have shown that there are micropores in the oxide 1 nm in diameter (33). This probably explains the growth rate, which is linear up to about 30 nm. Oxidant can diffuse to the interface through the micropores so that the growth is limited by surface reaction. The same oxides give poor breakdown statistics (21). On the other hand, no such micropores are observed in oxides grown in nitrogen with 10^{-4} ppm of water vapor. The growth rate of the wet oxide is parabolic. Without the micropores, the growth rate is limited by diffusion of oxidant through the oxide. The wet oxide has much better breakdown statistics.

There are different explanations for the correlation. Irene postulated that with the micropores, there was fluctuation of electric field in the oxide, with local high field regions giving enhanced injection and lower breakdown voltages (33). With growth in water vapor, the micropores may be filled by the OH groups. A more uniform electric field may be the result and thus better breakdown statistics. There is, however, another important variable: growth rate. The above reported wet oxide is also grown slower (21).

In dry oxygen growth, when the growth rate was reduced by using low oxygen pressure, good breakdown statistics were also reported (24). It is not surprising that under fast oxide growth, a looser oxide network with micropores is formed. Oxides grown in the linear growth regime may give poor breakdown. Growth temperature is another important variable. It was reported that lower temperature oxides had higher density (34) and higher optical index (35). For 22 nm oxides, oxides grown at 800°C have better breakdown properties compared to the ones grown at 900°C or 1000°C (36). Finally, the improved breakdown properties in wet oxides may also be the result of trapping and this will be discussed in more detail later. All the effects have to be studied in detail as the growth of very thin oxides requires much more critical control.

Osburn et al. have studied the reliability of silicon dioxide under accelerated thermal and field stress conditions (37,38). They reported an increase in the number of low field breakdowns with time, especially when aluminum was used as the top electrode (Figure 4). The increase is an exponential function of decreasing thickness and it is possible that aluminum gate devices with very thin oxides may fail in the field in a short time. This effect is probably related to reaction and diffusion of aluminum in the oxide. Aluminum has been reported to diffuse in silicon dioxide to a depth of 10 nm (39). The result may be exaggerated by the profiling process but a very thin oxide with an aluminum gate is potentially a reliability problem. The problem may be overcome by the use of a polysilicon gate. The same experiments on polysilicon gate capacitors showed that the degradation is much slower compared to aluminum gate and there was no change with oxide thickness, making it as reliable for a 10 nm oxide as a 50 nm oxide (38). Thus, for VLSI, the polysilicon gate process is important.

The use of a polysilicon gate does raise another problem. The very thin oxide must be able to withstand the deposition and diffusion of polysilicon. It has been reported that for arsenic diffusion, 4 nm oxide was sufficient to prevent diffusion of arsenic through the oxide into silicon (40). But it is possible that there is a certain amount of dopant diffusing into the oxide. Such diffusion may change the electrical properties of the oxide, causing trapping and other long term reliability problems. It may be even worse when metal silicide is used. Again, it is important to study the effects to fully evaluate the use of very thin oxides.

IV. Interface Properties and Trapping

There have been very limited reports on the density of fixed charge and interface traps for the very thin oxides. In such oxide systems, the oxide capacitance is high. A small change in flatband voltage gives a large change in charge density. Any uncertainty in the metal silicon work function difference gives a large error in fixed charge density. Similarly, the high oxide capacitance can give large error when the interface trap density is determined.

For very thin oxides, the dependence of the densities of fixed charge and interface traps on oxidation and annealing temperatures is similar to that of thick oxides (11,41). One important difference is the detrimental effect of nitrogen annealing is enhanced (42). Low fixed charge density cannot be attained and the fixed charge density is increased after a short anneal at 1000°C. At lower temperature, the increase in fixed

charge is delayed. No such fixed charge generation is observed when oxides are annealed in argon. As for interface traps, the reported trap densities for tunnel oxides have always been much larger than in thick oxides (11). Ogata et al. reported that interface trap densities were increased with decreasing oxide thickness (43). Homuchi et al. reported that interface trap densities were lower for higher temperature oxidation (23). These reported high densities could have been the result of lower temperature oxidation and improper annealing (41), but it may also be an intrinsic limitation in very thin oxides. The proximity of the gate electrode may also affect the interface traps. For lowest fixed charge and interface trap densities, a high temperature anneal in argon gives the best results. Besides fixed charge and interface states, the dielectric constant for very thin oxides also seems to be different (11,43) and it is changed by annealing (11). It is possible that there is a transition region with a higher dielectric constant. When the oxide thickness is reduced, the transition region contributes more to the total dielectric constant.

For trapping in the oxide, the dependence of electron trapping on oxide thickness has been studied (Figure 5) (44). The traps are distributed in the bulk of oxides and flatband voltage shift decreases as the square of oxide thickness. Very small voltage shift is expected for oxides less than 20 nm thick. However, this is only true when interface effects are ignored. Besides electron trapping in the bulk, interface traps are generated when hot electrons are injected (44,45). With the reduction in bulk trapping, the interface trap charge dominates the capacitance change. The charge in the interface traps tends to give a larger shift in the inversion voltage compared to flatband (Figure 6) (45). Even though the flatband shift may be small, there is still a large shift in the threshold voltage in MOSFETs. Under suitable annealing conditions, electron traps in oxides can be reduced to very low levels (45). It is postulated that the annealing decreases the density of water related centers, thus reducing trapping. Preliminary results indicate that the annealing is more efficient for thinner oxides, and a shorter time is needed to reduce the trapping (46). It has been shown that the water related centers are responsible for the degradation in the memory window in EAROMs (3). It may be possible to significantly improve the number of write and erase cycles before the collapse of the memory window when very thin oxides are used.

It has been demonstrated recently that electron traps play an important role in controlling breakdown in oxides (47). Breakdown is initiated in localized regions with enhanced injection due to high localized fields. If there are electron traps in the oxide, the traps are filled by injected electrons causing a local charge build up. This build up of negative charge produces an opposing field, lowering the local high field and choking off the enhanced injection. The number of local breakdowns is thus reduced. In fact, this effect may play a very important role in the reported difference in breakdown properties between dry and wet oxides. Making use of this effect, it is possible to introduce traps selectively to improve breakdown and yield of very thin oxides.

V. Radiation Effect

The dependence of radiation damage on oxide thickness has been studied for thicker oxides. The flatband or threshold voltage shifts were reported to be proportional to either d_{ox}^2 (48) or d_{ox}^3 (49). When extrapolated to below 20 nm, very small flatband

shift is expected. In fact, it was reported that there was no change in flatband voltage when the oxide was thinner than 15 nm (Figure 7) (50,51). At the same time, it was reported that the recovery time of hardened oxides to radiation was significantly shorter for thinner oxides (51). Also, electron beam damage experiments on very thin oxides showed that there was little generation of interface traps (52). All these show that very thin oxides are highly resistant to radiation damage.

The results on radiation damage contradict hole trapping experiments. Hole traps are localized close to the silicon-silicon dioxide interface. They should still be present when the oxide thickness is reduced. This is indeed the case because there is still significant hole trapping for 10-20 nm oxides (53,54). The advantages of very thin oxides in radiation damage may be due to the very small volumes for carrier generation. Another possible explanation is the holes that are generated within tunneling distance of the two electrodes recombine with direct tunneling electrons before they are transported and trapped at the interface.

Most of the work on radiation damage was on devices with aluminum gates. As mentioned before, aluminum gate devices are not desirable in very thin oxides. The effect of radiation on polysilicon gate on very thin oxides has to be studied in detail to determine if the advantages for aluminum gate devices are carried over. Future VLSI circuits are going to be using electron beam or X-ray lithography and it is very important to understand the effect of radiation on very thin oxides prepared under various processing conditions.

VI. Thermal Silicon Oxynitride

There were various attempts to prepare silicon nitride by direct reaction of nitrogen or ammonia with silicon at high temperatures (55,56). All earlier attempts failed to produce uniform and amorphous films. Ito et al. reported the first success in the growth of nitride films by carefully excluding oxygen and water vapor from the system (12). A few ppm of either oxidant will inhibit the growth of the nitride. Amorphous films up to 10 nm can be prepared. In their published AES spectra, there is a large oxygen peak and the films should more accurately be called silicon oxynitrides. Since then the experiments were repeated in different laboratories (14,57). With the minimum oxidant impurities, oxynitride films up to 4.5 nm were grown. The growth is self limiting. The oxynitride forms a very good diffusion barrier, preventing the in-diffusion of reactant to the interface for further growth. Recently, Ito reported that it is possible to convert silicon dioxide into oxynitride by direct nitridation of the oxide (58,59).

Oxynitrides offer many advantages over silicon dioxide as very thin insulators. It is a very good diffusion barrier as is demonstrated by the self limiting growth. Mobile ions are not a problem and Ito et al. reported that there is no degradation with deposition and diffusion of polysilicon gates (13). Oxynitride has a high dielectric constant (15). This would give a higher transconductance compared to oxide MOSFETs and minimize the short channel effect (15). It also appears to be electrically very uniform as there is no low field localized breakdowns. Because of this, it can sustain a high current flow before destructive breakdown. Finally, oxynitrides possibly offer the opportunity of tailoring the energy band-gap of the insulator to optimize the writing and retention

characteristics of EAROMs (60). This is accomplished by grading the insulator from oxynitrides to oxides.

Oxynitrides do have some disadvantages. The most serious one is the high temperature and length of time it takes to grow films of usable thickness. This is not very desirable for VLSI processing. Progress in this direction must be made before the use of oxynitrides can find wider acceptance. One solution may be some form of plasma assisted process. Another disadvantage is the lower bandgap of oxynitrides compared to oxides. This may enhance the hot electron problem.

Very little is known about the physical and electrical characteristics of oxynitrides. Problems, like reliability, interface effects, trapping and radiation effects must all be studied in detail to fully realize the potential of this interesting alternative insulator.

VII. Conclusions

The various problems and advantages of the use of very thin insulators are reviewed. In the present work, only the insulator and interface properties are discussed. There are other effects like channel mobility and gain of MOSFETs in practical VLSI devices which are not discussed here. The most important problems in the use of such thin insulators are breakdown and yield. It may be improved by further understanding of the growth process and the selective use of electron traps. The other major problem is the use of polysilicon gates in such thin insulators. Deposition and diffusion of polysilicon gates, together with resistance to radiation are areas that have to be studied.

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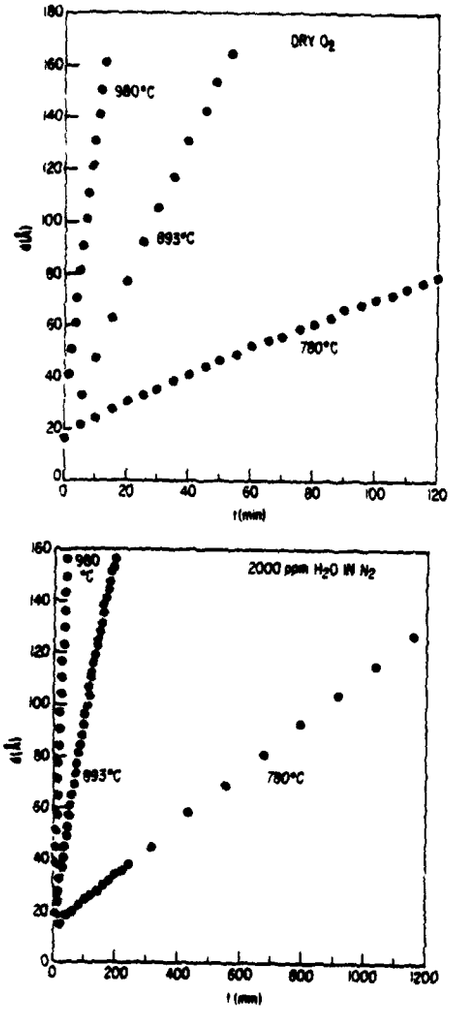

Figure 1. SiO_2 film thickness, d, vs. time of oxidation, t, at 780°, 893° and 980° in dry O_2 and 2000 ppm H_2O in N_2 as obtained from automatic ellipsometer (from Ref. 21).

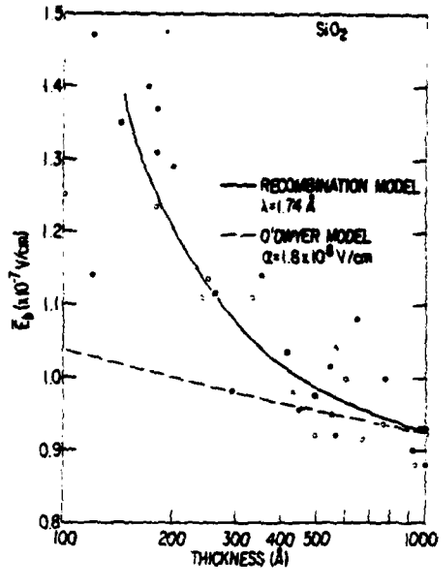

Figure 2. Dielectric strength as a function of thickness of an SiO_2 layer (from Ref. 31).

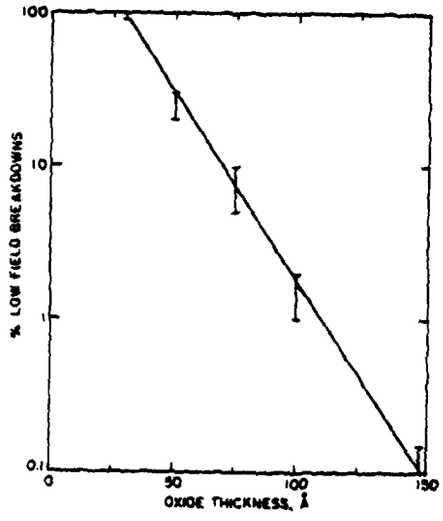

Figure 3. The % low field breakdown vs. oxide thickess (from Ref. 24).

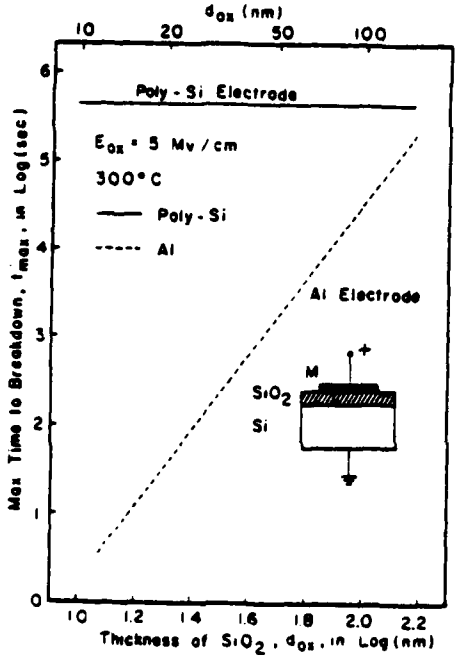

Figure 4. Maximum time to breakdown vs. thickness of SiO_2 with Al and Si electrodes in MOS capacitors (from Ref. 2).

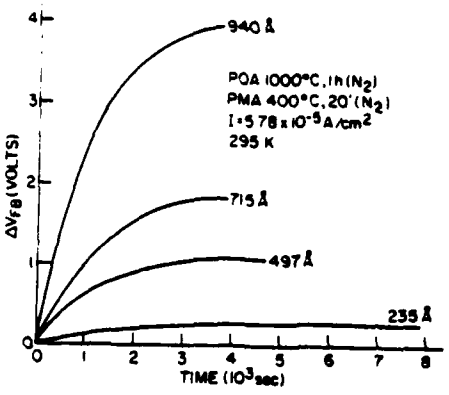

Figure 5. ΔV_{FB} as a function of time for various oxide thicknesses for avalanche injection of electrons (from Ref. 44).

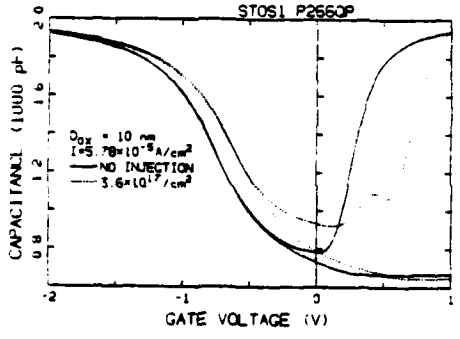

Figure 6. 1 MHz and quasi-static capacitance curves before and after injection of $3.7 \times 10^{17}/cm^2$ of electrons in a 10 nm oxide with aluminum electrodes.

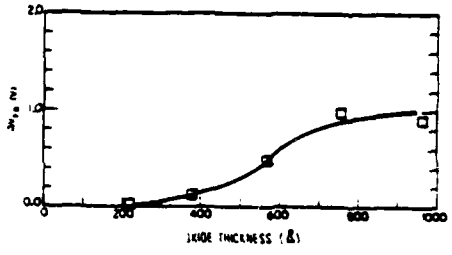

Figure 7. ΔV_{FB} as a function of oxide thickness for as-grown oxides following 0.5 M rad Co^{60} irradiation at room temperature and at applied field of 1 MV/cm (from Ref. 51).

Two Carrier Nature of Interface State Generation in Hole Trapping and Radiation Damage

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ABSTRACT

In hole trapping and radiation damage in silicon dioxide, a characteristic interface state peak is present. It is shown by the present work that the interface peak is due to trapping of holes at the silicon-silicon dioxide interface and the subsequent capture of injected electrons by the holes. It is postulated that dipolar complexes are formed which give rise to electronic states at the interface. Similar dipoles may be responsible for neutral traps in the bulk of oxides after irradation.

It has been reported that one of the results of radiation damage and hole trapping in silicon dioxide is the generation of interface states at the silicon-silicon dioxide interface[1-5]. The process of interface state generation can actually be divided into two steps[4]. The first step involves the transport to and the trapping of holes at the interface[4,5]. Holes can be generated by electron beam[1,6], gamma-ray[2], X-ray[7], vacuum ultra violet light[2,6-9] or any form of radiation that has sufficient energy to generate electron-hole pairs in oxides. They can also be generated by high field stress in oxides[5,7,10]. Holes in the bulk of the oxide are transported to the silicon-silicon dioxide interface through some form of hopping process characterized by very low mobility[4,11]. Part of the holes recombine while a fraction of them are trapped near the interface[4-9]. These trapped holes give rise to a positive charge distribution near the interface and are reflected by a shift of the C-V curve in the direction of negative voltages.

Once the holes are trapped near the interface, there is the much slower second step of interface state generation[3-5]. The generation has been studied in two different ways. Hu et al. generated and trapped holes by high field stress at liquid nitrogen temperature. They then measured the generation of interface states when the samples were warmed up to room temperature or above[5]. They observed a one to one relationship between interface states generated and holes trapped over a very long time. Winokur et al. measured the build up of interface states as a function of electric field and temperature after oxides were irradiated by electron pulses from an electron linear accelerator[3,4]. They observed that the generation of interface states was enhanced by both higher field and higher tempertaure. They explained the effect by the release of energy by trapped holes. The released energy was sufficient to break bonds to give rise to interface states[4]. The interface state spectrum was not reported in the above experiments, but the interface states generated after radiation damage had a broad peak approximately .25 ev above midgap towards the conduction band. These interface states were uaually measured by the quasi-static capacitance technique[1,3]. The peak was observed in oxides that were damaged by different kinds of radiation larger than a certain dosage[1], and it was believed to be characteristic of radiation damage[12].

In the present work, the processes of hole trapping and interface state generation are studied. Instead of using high energy radiation which generates both holes and electrons, only holes are injected into the oxide by avalanche injection from the silicon substrate[13]. By this technique, only the effect of hole trapping is studied, avoiding complications due to electrons. The process of hole injection is similar to the first step of hole generation described above. After hole injection and trapping, the interface state peak described above was not observed. There was only an increase in the background interface states. An attempt was made to neutralize the holes by injecting electrons by internal photoemission[7]. As the holes were neutralized, the C-V curve shifted in the positive voltage direction. Unexpectedly, however, as electrons were injected, the interface density was increased and the peak characteristic of radiation damage appeared. These results indicate that both trapped holes and trapped electrons are necessary to give rise to the build up of interface state peak and that the holes are not simply neutralized. All the previous experimental observation of field and temperature dependence of interface state generation might be explained by the electron injection model.

The wafers used in the present experiments were n-type, <100> in orientation and had resistivities of .1 to .2 ohm-cm. The oxides were all dry oxides. Some of them were pulled from the furnace in oxygen to ensure radiation hardness[13]. Others were annealed in nitrogen or argon for times ranging from 20 minutes to 17 hours to give oxides with different degrees of radiation hardness[13-15]. The oxide thickness were in the range of 10 nm to 100 nm and oxidation temperatures were from 800°C to 1000°C depending on the oxide thickness. Aluminum 13.5 nm thick was used as the top transparent electrode in simple MOS capacitors for all the measurements. The transparent electrodes were necessary for internal photoemission experiments. The system used for avalanche injection of holes was the same one used for avalanche injection of electrons or holes described previously[13,16]. A deuterium lamp was used for electron injection and a Corning glass filter was used to limit the light energy to less than 5 ev. The filter was necessary to prevent the injection of holes. The dependence of the

density of hole traps on processing followed the dependence of radiation hardness on processing[13-15]. The present reported results were observed on all the oxides.

Figure 1 shows the high frequency and quasi-static capacitance curves before and after injection of $10^{15}/cm^2$ holes and then after a subsequent injection of $6x10^{14}/cm^2$ electrons for a 50 nm oxide. The result is typical of what was observed in ten oxides of different thickness and prepared in different ways. After hole injection, the high frequency curve is shifted in the negative voltage direction and this voltage shift is proportional to the density of trapped holes. There is also some interface state generation as can be seen from the quasi-static curve. After the injection of electrons, the high frequency curve is shifted back in the positive voltage direction to almost the original curve. This is complicated by the distortion in the curve because of interface states. There is a distinct feature in the quasi-static curve indicated in the figure by an arrow. That is due to the interface state peak observed in radiation damage. The interface state spectrums can be calculated from the capacitance curves and the results are plotted in figure 2. There is increase in interface states after hole injection but the characteristic peak is not present. The falloff in interface state density close to the conduction band is due to limitations of the measurement in that region. After electron injection, a distinct interface state peak appears, the same that is observed in radiation damage. The peak height is a monotonic function of number of trapped electrons. The kinetics of electron trapping were analyzed and were shown to be due to capture by coulombic attractive positive charge centers. The capture cross section is very large and it decreases with increasing electric field in the oxide[7,17]. The only positive charge centers present in the oxide are the holes. Thus the shifting of the C-V curves is due to the capture of electrons by the holes, compensating the charge. The electrons can be injected from either the aluminum or the silicon and the same results were obtained. The simple conclusion is that electrons are captured by the holes. It is not the simple recombination process that is observed in crystalline silicon. Instead, electrons and holes may recombine, releasing energy in such a way as to induce structural change at the interface to give rise to interface states. This is the reverse of what Ma et al. proposed as the

mechanism for RF annealing[18]. Another possible explanation is that electrons may be bound to holes in dipolar complexes to give electronic states at the interface.

The above result can be used to explain the interface state generation observed previously. When there is positive charge trapped near the silicon-silicon dioxide interface, electrons in silicon can tunnel directly into the charge centers depending on the relative energy levels. The field and temperature dependence reported on the interface state generation after electron beam pulses[3,4] can be qualitatively explained by such tunneling. The increase in field simply enhances the tunneling of electrons by making more of the trapped hole levels available to tunneling electrons, and the tunneling barrier is lowered by the field. This also explains the recent reported observation that interface states were not generated when the field was reversed by switching to negative gate bias voltage, after holes were transported to the interface under a positive bias[19]. It was impossible for electrons to tunnel in directly from the metal side because of the oxide thickness and the field was too low for Fowler-Nordheim tunneling. On the silicon side, the field opposed the tunneling of electrons from silicon into holes in the oxide. There is no such limitation if electrons are injected by internal photoemission over the interfacial energy barriers. As for the temperature depedence, there are two possible explanations. If the energy levels of the holes lie above the conduction band of silicon, the tunneling would be thermally assisted. When holes are trapped at liquid nitrogen temperature[5], there would be very little thermally assisted tunneling of electrons from silicon into the oxide. Going to room temperature or above increases thermally assisted tunneling and thus generates interface states. Another explanation is some thermal energy is needed in the formation of interface states.

Under normal conditions in radiation damage, there are electrons and holes generated. Some of the electrons are captured by the trapped holes to give the interface state peak. The same process may also occur in the bulk of oxides. Aitken proposed that radiation induced neutral traps in the bulk of oxides were due to dipoles[20,21]. It was based on the experimental

observation that densities and location of both neutral electron and hole traps in the bulk of irradiated oxides were the same and that they might be the same traps but dipolar in nature[21]. This can be explained by the following simple model. Intrinsic hole traps exist in the bulk of oxide or at the interface as strained bonds. In a simple minded picture, a hole is a broken bond in an amorphous oxide network. Holes can move from one unstrained bond to the next under an electric field if there is no change in the unstrained bonds in the process. But if a hole gets to a strained bond and enters into a lower energy metastable state by deforming it further, the hole may be trapped. These trapped holes have very large capture cross section for the capture of electrons, which are also generated and present in the oxide. When the trapped holes capture electrons, the deformed bonds cannot be restored to original states. In this way neutral traps are formed in the bulk and interface states are generated at the interface. The properties of the neutral traps thus favor the model of an electron and a hole forming a dipolar complex to give an electronic state. However, the model for recombination induced structural change cannot be ruled out completely. From previous work on damaged oxides, the interface states at the peak are acceptor states[22]. This means that they are neutral when empty and negative when occupied by electrons. This may have some significance in the study of the nature of the interface state.

It must be pointed out that there may be two kinds of positive charge at the interface. The first are the holes trapped at the interface as described above. The second is the anomalous positive charge that was observed in electron trapping experiments[16,23]. All evidence so far indicates that the anomalous positive charge is generated as a result of trapping of electrons at water related centers in the bulk of the oxide[16]. After the trapping, some transport process, which may be exciton or hydrogen[9,24], causes the generation of slow interface states at the interface. The slow interface states are donors and are positively charged when empty[16,21]. The properties of the anomalous positive charge have been investigated and will be reported in a future paper[25]. In the process of high field stress or radiation damage, there are electrons as well as holes flowing in the oxide and the interaction of the electrons with water

related centers, which are present even in dry oxides, may give rise to some anolmalous positive charge. The water related centers have small capture cross sections in the 10^{-17} to 10^{-18} cm^2 range[16] and densities $\geq 10^{11}/cm^2$. The anolmalous positive charge are observed after passage of $10^{16}/cm^2$ of electrons[25]. Weinberg et al. have shown that positive charge appeared at the silicon-silicon dioxide interface even when the applied field opposed the transport of holes to the interface and that the effect was enhanced in wet oxides[22]. So, in most of the reported results in the literature it must be understood that both trapped holes and anomalous positive charge may be present at the interface. The effect may be more significant when wet oxides are used. In the present experiments, no electrons are injected during the first step of hole injection. Too few electrons are injected by internal photoemission to interact with water related centers. Therefore, there is no generation of anomalous positive charge.

In conclusion, it was shown that the interface state generation in radiation damage and hole trapping is due to the injection of electrons. They are captured by trapped holes. One possible result is the formation of dipolar complexes which give rise to electronic states at the interface. Another possibility is the recombination of the electrons and holes releases energy to form defect interface states. The result can be used to explain the field and temperature dependence reported by other workers. It is also very important for the understanding of the electronic states at the interface and may contribute to solving the problem of degradation in devices due to radiation damage. Further experiments are now being planned to study the process and the interface states in more detail.

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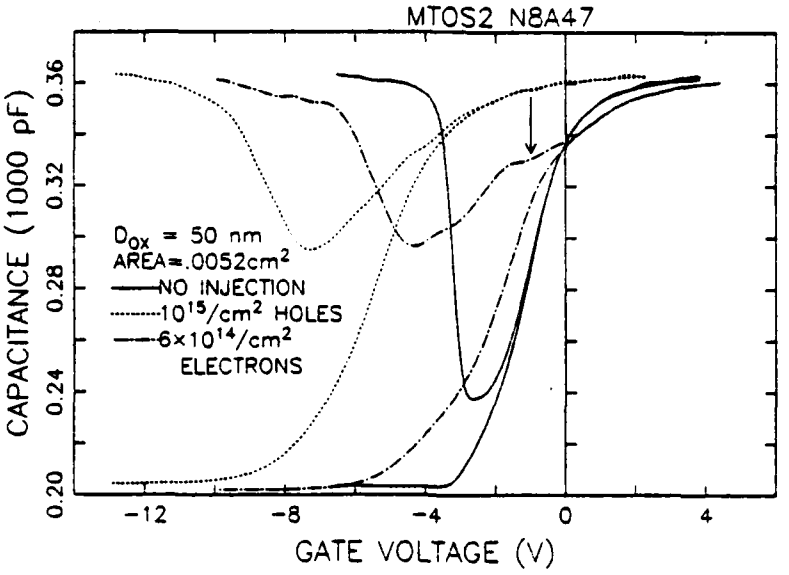

Figure 1 High frequency (1 MHz) and quasi-static capacitance curves for before and after hole injection and then after subsequent electron injection. The hole injection was by avalanche of the silicon substrate at a current level of $5.4 \times 10^{-8}/cm^2$ for 3000 seconds giving a total of $10^{15}/cm^2$ holes. The electron injection was by internal photoemission at a current level of approximately $4.8 \times 10^{-8}/cm^2$ under a negative oxide field of about 2 MV/cm. The injection time was 2000 seconds giving a total of $6 \times 10^{14}/cm^2$ electrons. The feature in the third quasi-static curve marked by an arrow is due to an interface state peak.

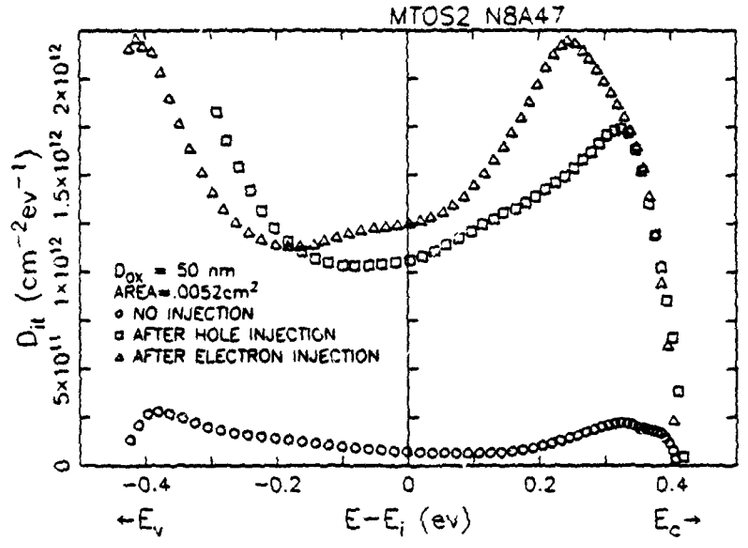

Figure 2 Interface state spectrums calculated from the high frequency and quasi-static capacitance curves in figure 1. The feature in the quasi-static curve after electron injection shows up as an interface state peak at .25 ev above midgap.

Review of RIE Induced Radiation Damage in Silicon Dioxide

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ABSTRACT: Radiation damage in silicon dioxide films exposed to Reactive Ion Etching (RIE) has been investigated. Capacitance-voltage (C-V) and photocurrent-voltage (photo I-V) techniques were used to monitor charge trapping and the location of trapped charge after the films were incorporated into MOS capacitors. Bulk, neutral trapping sites caused by penetrating radiation were observed in oxides exposed to CF_4, CF_4+H_2 and O_2 plasmas, although the number of radiation induced traps was somewhat lower in oxides etched in CF_4+H_2. The neutral trapping centers are removed by a 600°C anneal in forming gas. An additional trapping layer within 10 nm of the surface of the oxide was detected in oxides exposed to O_2. These traps which are primarily associated with atomic displacement damage caused by the penetration of ions ($\lesssim$ 400 eV) require a 1000°C anneal for their removal. Blanket etched films were also used to study the trapping characteristics of the bulk, neutral traps as a function of position in the reactor, rf peak-to-peak voltage, and pre-RIE high temperature annealing. The ability of gate electrode materials to shield an underlying oxide during RIE was also tested. It was determined that aluminum and n^+ polysilicon are effective in shielding oxides from RIE induced radiation damage.

I. Introduction

Reactive Ion Etching (RIE) is a directional, dry etching technique that is capable of etching densely packed micron dimension structures. RIE is used at several levels of processing FET chips including definition of recessed oxide isolation, polysilicon gate electrodes, and contact holes to polysilicon and diffused regions[1,2]. The directional etching that is required for patterning at these small dimensions is obtained by loading wafers on an rf cathode and etching in a low pressure discharge of a gas such as CF_4[3]. RIE is, however, carried out in a radiation environment; substrates are subjected to bombardment by energetic electrons, ions and photons. The radiation present during RIE creates electron traps in silicon dioxide which, if not annealed, produce a shift in the threshold voltage during the operation of the device. For this reason, experiments have been carried out to characterize electron traps in blanket etched oxide films, determine the dependence of these traps on RIE parameters, and evaluate the ability of gate electrode materials to shield underlying oxide from RIE damage. RIE induced radiation damage was studied by etching silicon dioxide films in CF_4 and CF_4+H_2, or by exposing them to an O_2 plasma which is used to strip resist and clean wafers. Trapping was characterized by incorporating the etched oxide into an MOS device and injecting charge into the conduction band of the oxide by avalanche injection. The numbers and cross-sections of the traps, the density of trapped charge, and the centroid of the trapped charge distribution were determined by C-V and photo I-V techniques. A discussion of these measurement techniques as well as a review of previous work in the area of electron trapping in silicon dioxide appears in reference 4. Traps are introduced by impinging ions and photons. Ions are accelerated to the substrate from the plasma by a dc voltage of ~400V. High energy photons are produced when secondary electrons strike ground planes. Energetic electrons in the plasma do not contribute to RIE damage because the cathode is biased negatively. Electron traps produced in silicon dioxide

by ions and photons in the RIE reactor are shown schematically in Fig. 1. Ions which have significant energies are implanted into the oxide film. The atomic displacement damage caused by the ions as well as the implanted ions themselves can form trapping sites for electrons or holes. High temperature annealing (1000°C in N_2) removes the atomic displacement damage, but trapping sites related to the implanted ions are still present[5]. Ions and high energy photons generate positively charged traps (trapped holes) and uncharged (neutral) sites[4,6-9]. The trapped holes are generated when electron-hole pairs are created in the oxide by ionization across the bandgap with the energetic particles or light, and some of these holes are captured from the oxide valence band into energetically deep trapping sites, near the silicon-silicon dioxide interface[9]. These trapped holes will not be considered further because they are removed from aluminum gated structures by a low temperature anneal (400°C)[7]. The neutral centers which can capture electrons are also believed to be created by the bandgap ionization process, but they are more difficult to anneal. They require a 600°C anneal and therefore cannot be removed when Al electrodes are in place[7].

In this work, electron trapping in silicon dioxide was studied as a function of etching gas, position of substrates, gas pressure, and rf voltage. In addition, the ability of gate electrode materials to shield an underlying oxide from RIE radiation damage was evaluated by etching silicon dioxide films masked with Al or n^+ polysilicon patterns.

II. Experimental

A. RIE System

The Reactive Ion Etching system used in this work is shown in Fig. 2. The substrates were loaded onto an 18 cm diameter aluminum plate. The aluminum plate was mechanically and electrically connected to the water cooled copper rf cathode. A perforated anode plate which was attached to the grounded chamber was placed 3.3 cm from the cathode in order to catch sputtered aluminum before it can be scattered back onto the substrate. A perforated

plate was used so that wafers could be monitored visually during etching, and also to ensure an adequate and uniform supply of etchant in the vicinity of the wafers. The chamber was evacuated with a 6 inch oil diffusion pump and then backfilled to establish a dynamic pressure of 3.33 Pa (25 millitorr). During etching, 0.25 W/cm^2 is delivered to the cathode. Under these conditions, the peak-to-peak voltage is 800 V. The dc voltage at the cathode is approximately one half of the peak-to-peak voltage[10]. The etch rate of silicon dioxide in CF_4 is approximately 50 nm/min.

B. Sample Preparation

Nominally dry, thermal oxide films of 150 nm thickness were grown on boron doped, <100> orientation, 0.1 to 0.5 Ω-cm resistivity, p-type silicon substrates. The oxide films were then exposed to a CF_4, CF_4+H_2, O_2 or Ar plasma. The films exposed to the CF_4 and CF_4+H_2 plasmas were etched back to approximately 100 nm. Other films were exposed to O_2 and Ar plasmas for 1 to 10 minutes. The wafers were then cleaned to remove metals and hydrocarbons from the surface of the oxide in alkali and acid peroxide solutions using a procedure similar to that used by Irene[11], but without HF. Some wafers received a buffered HF dip at this point in order to remove approximately 10 nm from the surface of the oxide. After cleaning, some wafers were annealed in a nitrogen ambient for 30 minutes. Annealing temperatures ranged from 600 to 1000°C. Circular aluminum dots, 13.5 nm in thickness and 5.2×10^{-3} cm^2 in area, were then evaporated in vacuum from resistively heated tantalum boats or rf heated crucibles. Finally, the backs of the wafers were stripped and metallized, and a forming gas anneal at 400°C for 20 minutes was carried out.

C. Techniques

To investigate the enhanced electron trapping characteristics of silicon dioxide films exposed to plasmas in an RIE system, avalanche injection[12,13] and internal photoemission[14-16] techniques were used to inject electrons from the contacts of the MOS structures into the

oxide. The experimental apparatus for avalanche injection[17] and internal photoemission[18] have been described in other publications. As the electrons traversed the film in the presence of an applied electric field, some of the carriers were trapped into sites created during RIE conditions. This trapping was not particularly sensitive to the mode of carrier injection: avalanche injection from the silicon or internal photoemission from the aluminum or silicon. The trapping rate was not particularly sensitive to the average field in the oxide layer which is consistent with the weak field dependence of the capture process for radiation induced neutral traps recently reported by Ning[8]. This weak field dependence is in contrast to the strong field dependence of electron capture on trapped holes[4,8,9].

The buildup of this trapped charge was sensed through the internal electric field it generates near the contacts by the capacitance-voltage (C-V)[19,20] and photocurrent-voltage (photo I-V)[9,21,22] techniques which are well described in the literature. The voltage shifts between the C-V curves depend on the product $\bar{x}Q$ where Q is the charge per unit area and $\bar{x}$ is the centroid of the trapped charge in the oxide layer measured with respect to the aluminum-oxide interface[19,20]. The voltage shifts between photo I-V data for both positive and negative polarity allow separate determination of $\bar{x}$ and Q[9,21]. The combination of the C-V and photo I-V techniques can also be used to separate trapping at the silicon-silicon dioxide interface from trapping in the bulk of the oxide[9,21,22]. Also by studying charge buildup as a function of time, electron capture cross-sections σ_c and trap densities N_t can be determined[4]. These quantities ($\bar{x}$, Q, σ_c, and N_t) are used to characterize the different traps created by RIE.

III. Results and Discussion

A. CF_4 and CF_4+H_2 Plasmas

C-V and photo I-V data characteristic of oxide films etched in a CF_4 plasma with the samples placed on the cathode are shown in Figs. 3-5 before and after some of the trapping

sites were charged by internal photoemission or avalanche injection. The C-V flatband voltage shift ΔV_{FB}[19,20] and the average photo I-V voltage shifts for positive and negative gate polarity[9,21] (ΔV_g^+ and ΔV_g^-, respectively) are recorded in the figure captions. These data are characteristic of a bulk oxide negative trapped charge distribution with some slight increase in trapping near the aluminum-oxide interface[21,22]. From the values for the average positive and negative photo I-V shifts and the photo I-V relationship $\bar{x}/L = (1-\Delta V_g^-/\Delta V_g^+)^{-1}$ where L is the total oxide thickness, a value indicative of bulk oxide charge ($\bar{x}/L \lesssim 0.5$) is obtained as listed in the figure captions. In addition, the centroid of the trapped charge distribution was determined to be independent of the injection interface and the number of injected carriers.

Figure 6 shows the areal trapped electronic charge buildup in the oxide layer as a function of the number of injected electrons per unit area for a sample etched in CF_4 and a sample from the same batch that was not exposed to RIE. Clearly the etched film shows enhanced trapping. These type of data were also used to determine the capture cross-sections and the trap densities. The electron-capture cross-sections for these traps have values between 10^{-14} and 10^{-17} cm^2 with areal trap densities varying between 10^9 and 10^{11} cm^{-2}..

In another experiment H_2 was added to CF_4. This experiment was suggested by speculation that the neutral traps were created by breaking or relaxing bonds in the oxide lattice[6]. If correct, the diffusion of atomic hydrogen into silicon dioxide might anneal neutral traps in a way that is analogous to the reduction in dangling bond density in amorphous silicon by atomic hydrogen[23]. In Fig. 7 the volume density of trapped charge n is plotted as a function of avalanche injection time. Assuming a uniform distribution of trapped charges as suggested by ($\bar{x}/L \lesssim 0.5$), $n = 2\,\varepsilon\,\Delta V_{FB}/qL^2$, where ε is the low frequency permittivity of SiO_2 and q is the magnitude of the charge on an electron. The data show that the addition of H_2 does lead to a reduction in trapped charge when compared with an oxide etched in CF_4

alone. A peak-to-peak voltage of 810 V was measured. This value is slightly higher than that measured during RIE in CF_4. While this effect of adding H_2 is reproducible and consistent with annealing of traps by atomic hydrogen, it was not possible to reduce trap density by introducing hydrogen in other ways. Trapping was not reduced by exposing oxides to hydrogen plasmas before or after RIE in CF_4 or by annealing oxides in forming gas (90% N_2/10% H_2) at 1000°C before RIE in CF_4.

It was suggested earlier that the neutral traps were created in the relatively low energy environment by photons. To substantiate this view, substrates were loaded onto the grounded perforated plate with the oxide film facing away from the cathode. In this way, the oxide film is no longer subjected to bombardment by energetic ions. The oxide film is also protected from secondary electrons from the cathode by the silicon substrate. The oxide film is, however, still exposed to photons that are created when secondary electrons strike the walls of the reactor. Figure 8 shows that the oxide etched by RIE and the oxide exposed only to energetic photons show enhanced trapping relative to that measured in the control sample.

The rf power was varied in order to vary the rf peak-to-peak voltage. Etch times were increased as voltage was decreased so that the amount of oxide removed was constant. The purpose of this experiment was to determine whether the introduction of traps exhibited a threshold in the regime of power and pressure that is appropriate for RIE. As can be seen in Fig. 9, enhanced trapping was observed for all oxides etched by RIE even though rf peak-to-peak voltage was reduced by more than a factor of two, from 730 to 330 V. Thus, radiation damage is not avoided by etching for longer times at lower rf voltages. It was not possible to carry out RIE at lower voltages. RIE requires low pressures tc maintain vertical etching and a low pressure could not be sustained at voltages below 330 V. It is possible, however, to reduce voltage if the requirement for directional etching is suspended. For this experiment,

pressure was increased to simulate plasma etching. Oxygen was added to CF_4 so that a direct comparison could be made with oxides etched in a commercial barrel plasma etcher. The pressure of the CF_4+20%O_2 etching gas was increased to 0.5 Torr which results in an rf peak-to-peak voltage of 120 V. The trapping data (Fig. 10) show that neutral traps are not created during plasma etching or during etching under plasma etching - like conditions in the RIE system. For completeness, an oxide was etched by low pressure RIE in the CF_4+O_2 mixture to assure that the addition of O_2 was not the significant factor. As expected, this oxide shows the presence of neutral traps with a trap density that is approximately equal to that of an oxide etched in CF_4.

B. O_2 Plasma

Oxides placed on the cathode and exposed to an O_2 plasma displayed the C-V and photo I-V characteristics shown in Figs. 11-13. These data indicate that strong trapping occurs in a layer close to the exposed surface of the oxide. This trapping layer is created by the implantation of low energy (fewer than 400 eV) ions. From the photo I-V relationship and the values given for the average value of ΔV_g^+ and the maximum observed value of ΔV_g^-, the centroid of trapped charge is within approximately 10 nm of the surface. The electron-capture cross-sections for these sites have values ranging from about 10^{-14} to 10^{-18} cm^2 with trap densities $>10^{13}$ cm^{-2}. These are very efficient trapping centers with an initial capture probability (product of the capture cross-section and number of traps per unit area) of >50%. The trapping probability was deduced by measuring the ratio of the buildup of the number of trapped charges determined from C-V or photo I-V voltage shifts to the number of injected electrons.

To determine whether trapping occurred on implanted ions or on lattice damage created by implanted ions, the O_2 plasma was replaced by one of a chemically inert gas, Ar. Also oxides exposed to an O_2 plasma were annealed at 1000°C in N_2 for 30 minutes before they

were metallized. This high temperature anneal would remove lattice damage. No strong dependence on gas, O_2 or Ar was observed, but trapping was greatly reduced by the high temperature anneal. Both results indicate that most of the trapping sites in this thin layer of oxide are associated with atomic displacement damage.

The build-up of trapped charge was also determined as a function of time of exposure to O_2 or Ar under RIE conditions of pressure and voltage (25 mTorr and 400V, respectively). Charge trapping was essentially the same after 1 minute as after 10 minutes. The lack of dependence on time suggests that this damage must saturate in a short period of time due to the heavy bombardment of energetic ions. The number of positive ions incident on the sample in 1 min could be as large as 2.3×10^{17} cm^{-2} for 0.25 W/cm^2 delivered to the cathode with a dark space dc voltage drop of $\approx$400 V. If a sample exposed to O_2 was given a buffered HF dip to remove about 10 nm of oxide, the trapping associated with the ion-implanted region is no longer present as expected, but the bulk radiation-induced neutral traps are still present.

C. Gate Shielding

The purpose of experiments carried out with blanket oxide films is to understand the nature and parameter dependence of the neutral traps. During FET processing, however, the gate oxide is covered by the material that is used as a gate electrode. With this fact in mind, the ability of polysilicon and aluminum to shield an underlying gate oxide from the introduction of neutral traps was tested.

The procedure used to fabricate the samples begins with the same cleaning and oxidation steps described earlier. After the oxide is grown, a 350 nm thick film of silicon is deposited by chemical vapor deposition on some substrates and then doped n^+ by the deposition and drive-in of $POCl_3$. The polysilicon plus 50 nm of oxide is etched using patterned photoresist to delineate 32 mil diameter dots. On other oxidized substrates, 32 mil diameter, 400 nm

thick aluminum dots are evaporated by resistive heating. 50 nm of oxide is then etched by RIE in CF_4. Appropriate control wafers were included to determine background trapping in the oxide in order to provide a reference for the degree of shielding by the gate electrode and to provide a comparison with wet etching of polysilicon. The data in Fig. 14 show that 400 nm of aluminum does shield the oxide. The shielded oxide exhibits the same increase in trapped charge density as the control, while the unshielded oxide again shows enhanced trapping. The trapping data for oxides covered by polysilicon plus resist during RIE also show that the oxide has been effectively shielded (Fig. 15). The trapped charge density for the reactive ion etched structure is shown on an expanded scale with the trapped charge density obtained for a structure that was wet etched. The two samples show the same low density of trapped charge. In fact, the trapped charge density measured for both samples is almost half that measured on similar structures with Al gate electrodes (see Fig. 14). This reduction is attributed to a decrease in background oxide trapping as a result of the high temperature deposition and doping of the polysilicon films.

IV. Summary

~~The presence of trapping sites generated by RIE in CF_4 or by O_2 plasma cleaning of~~ oxide layers in RIE systems has been demonstrated. The traps introduced during blanket etching in CF_4 are bulk sites with a centroid equal to approximately one half of the thickness of the oxide. These traps are removed by a 600°C anneal and so are of concern only if an RIE step occurs after aluminum metallurgy is in place. The trap density is reduced by adding H_2 to the etching gas. Neutral traps were not introduced when the reactor was operated under plasma etching-like conditions. Using oxides patterned with polysilicon or aluminum, it was shown that silicon dioxide is effectively shielded during RIE by these gate electrode materials.

Oxide films exposed to an O_2 plasma to strip resist or remove hydrocarbon exhibited greatly enhanced trapping in a layer near the surface of the oxide. Trapping occurred predominantly on sites associated with lattice damage created by implanted ions. This damaged region is absent in oxide films etched by RIE in CF_4 and CF_4+H_2. Presumably damage is removed by etching as it is created. As expected, the trapping layer in oxides exposed to an O_2 plasma is removed by chemically etching approximately 10 nm of oxide in buffered HF.

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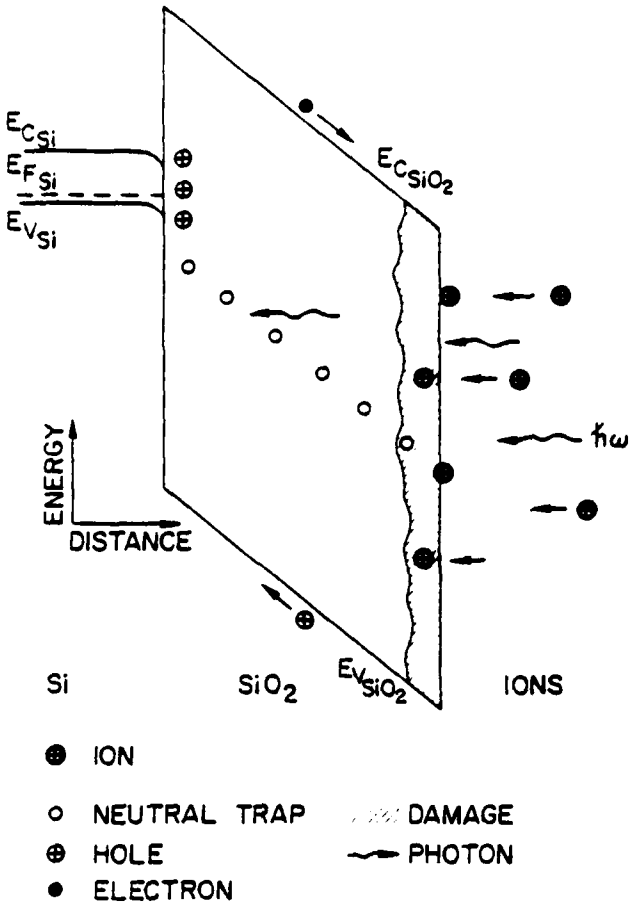

Fig. 1 Energy band diagram for thermal SiO_2 layer on an underlying silicon substrate exposed to low-energy positive ions and photons which are present in an RIE reactor.

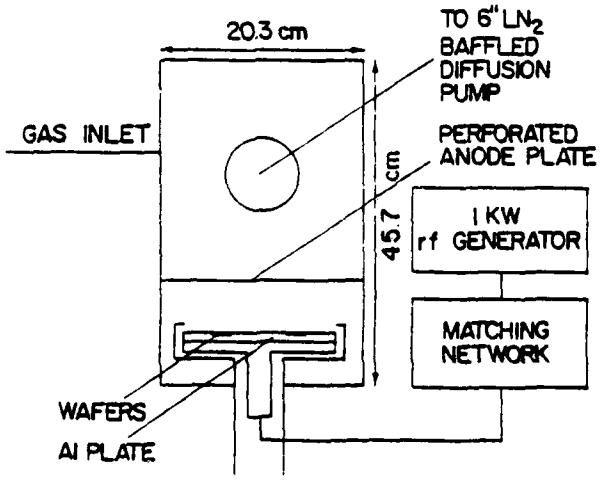

Fig. 2 Schematic of RIE Reactor

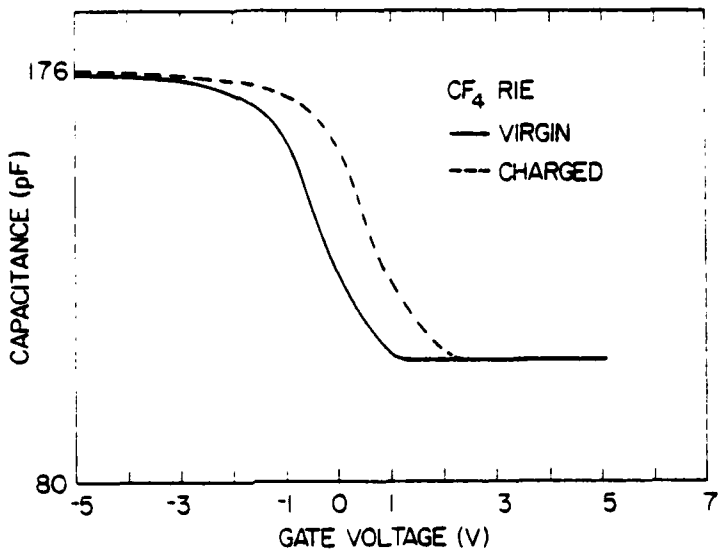

Fig. 3 High-frequency (1 MHz) capacitance as a function of gate voltage before and after charging of the radiation-induced neutral traps in the bulk of the SiO_2. The oxide layer of this sample was etched from 150 to 94.5 nm in a CF_4 plasma. Approximately 4×10^{15} electrons/cm^2 were avalanche injected into the SiO_2 layer from the Si substrate. The flatband voltage shift due to charging is $\Delta V_{FB} = 1.0 \pm 0.1$ V.

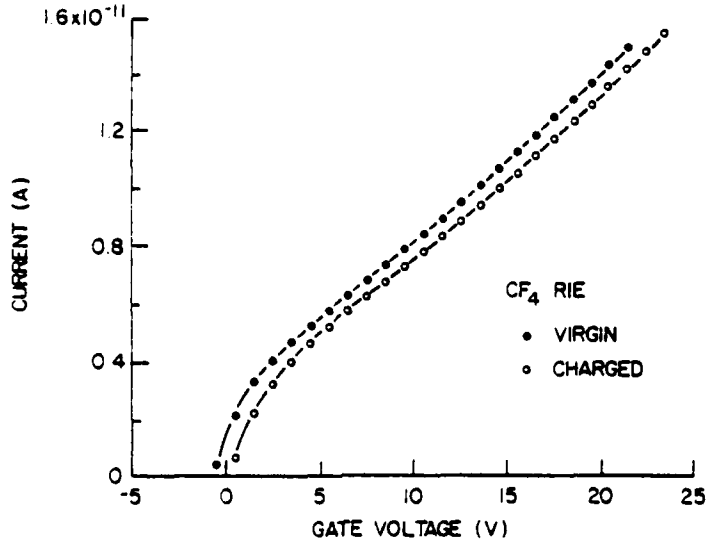

Fig. 4 Magnitude of the current measured in the external circuit for 5-eV light as a function of positive gate voltage (Si injecting) for the same sample before and after charging as in Fig. 3. The average positive photo I-V shift between these curves is $\Delta V_g^+ = 1.01 \pm 0.1$V.

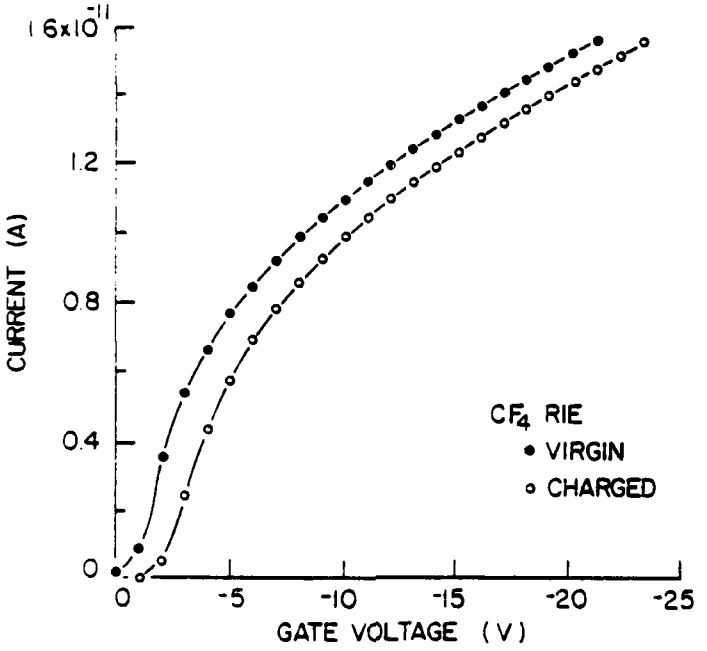

Fig. 5 Magnitude of the current measured in the external circuit for 4.5-eV light as a function of negative gate voltage (Al injecting) for the same sample before and after charging as in Fig. 3. The average negative photo I-V shift between these curves is $\Delta V_g^- = -1.7 \pm 0.1$V. The centroid determined from the photo I-V voltage shifts is 35 ± 3.5 nm.

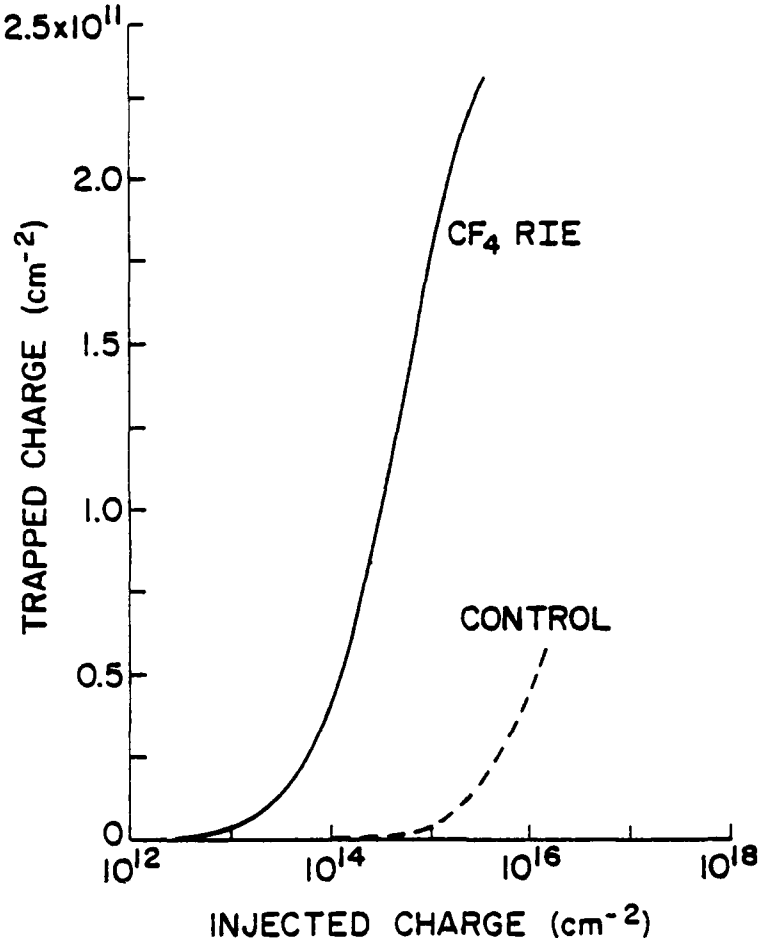

Fig. 6 The number of negative charges per unit area as a function of the number of injected electrons per unit area for a control and a sample similar to that used in Fig. 3. An avalanche current of $2x10^{-10}$ amps was used to charge the traps. The control had the same processing as the etched sample. The negative charge trapping in the etched oxide is due to the radiation-induced neutral centers, while that in the control is due to the neutral centers normally present in the oxide layer.

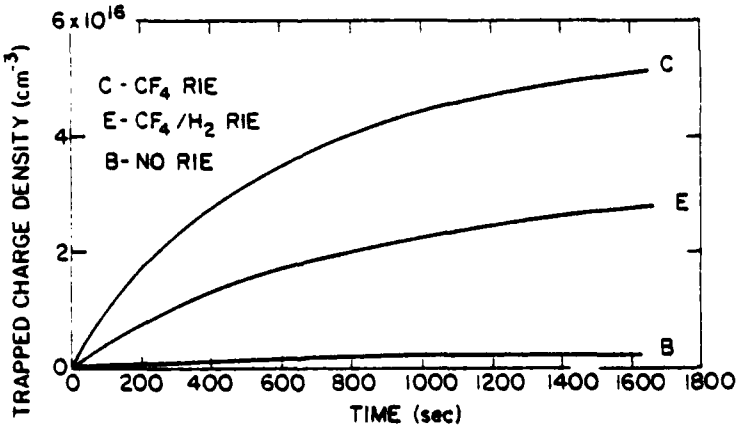

Fig. 7 Volume trapped charge density as a function of avalanche injection time for oxides exposed to RIE in CF_4 and CF_4+H_2. Constant avalanche current = $2x10^{-9}$ amps.

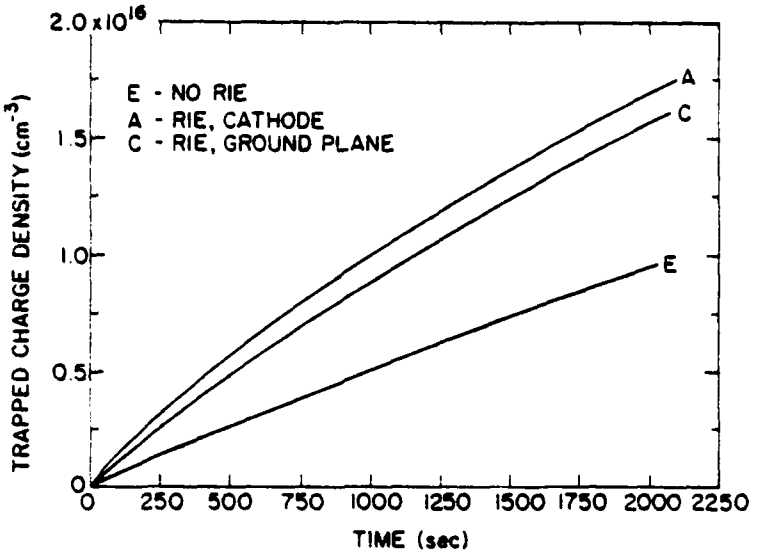

Fig. 8 Volume trapped charge density as a function of avalanche injection time for oxides exposed to RIE on the electrode and on a ground plane. Constant avalanche current = 8×10^{-9} amps.

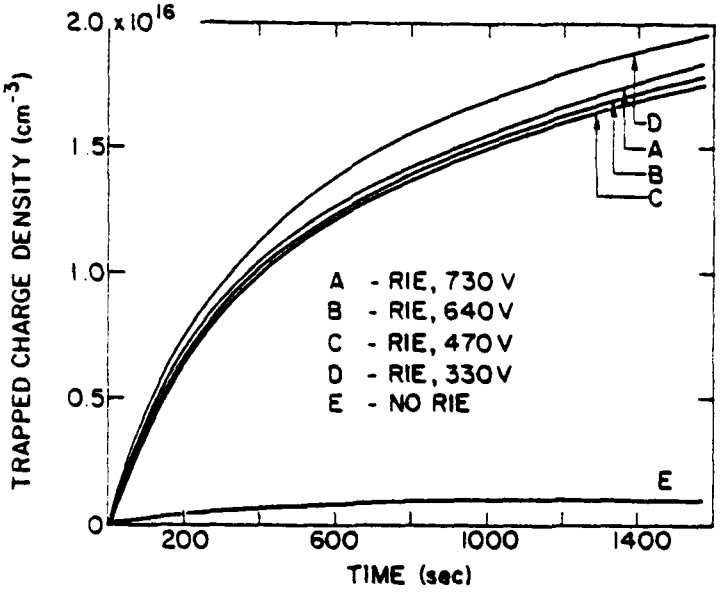

Fig. 9 Volume trapped charge density as a function of avalanche injection time for oxides exposed to RIE with rf peak-to-peak voltages between 730 and 330V. Constant avalanche current = 2×10^{-9} amps.

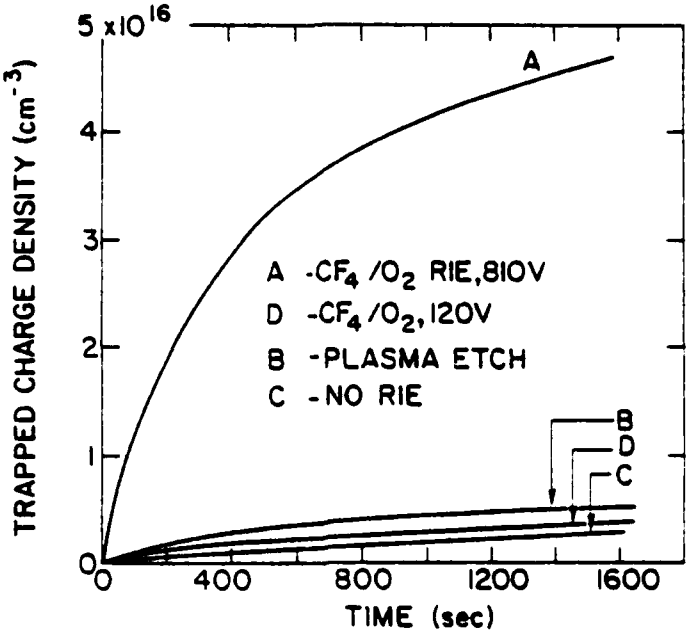

Fig. 10 Volume trapped charge density as a function of avalanche injection time for oxides exposed to RIE in CF_4+O_2, and plasma etching in RIE and barrel-type plasma reactors. Constant avalanche current = $2x10^{-9}$ amps.

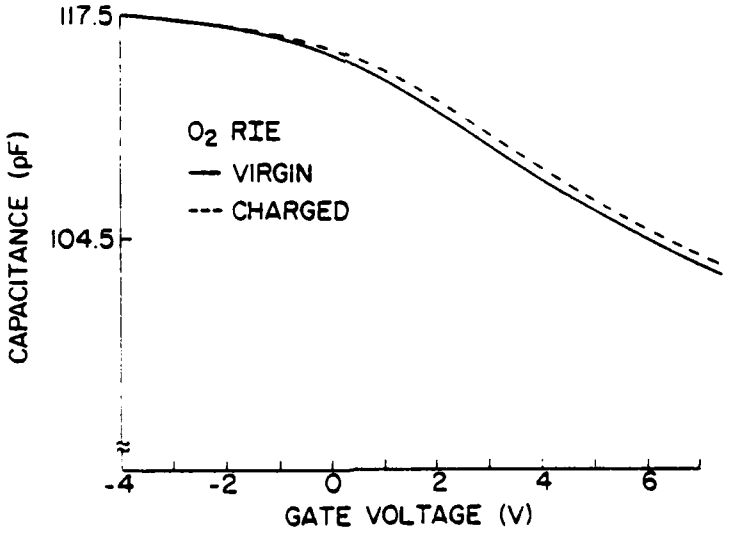

Fig. 11 High-frequency (1 MHz)capacitance as a function of gate voltage before and after partial electronic charging of some of the radiation-induced neutral traps in the bulk of the SiO_2 layer and traps near the exposed oxide surface caused by damage due to the ion implantation of oxygen. The oxide layer of this sample was exposed to an O_2 plasma for 10 min after which the SiO_2 was 145 nm thick. This sample had only a 400°C 20-min forming gas anneal after metallization. Approximately $2.5x10^{14}$ electrons/cm^2 were injected into the oxide film by internal photoemission from the aluminum electrode. The flatband voltage shift due to charging is $\Delta V_{FB}=0.4\pm0.1V$.

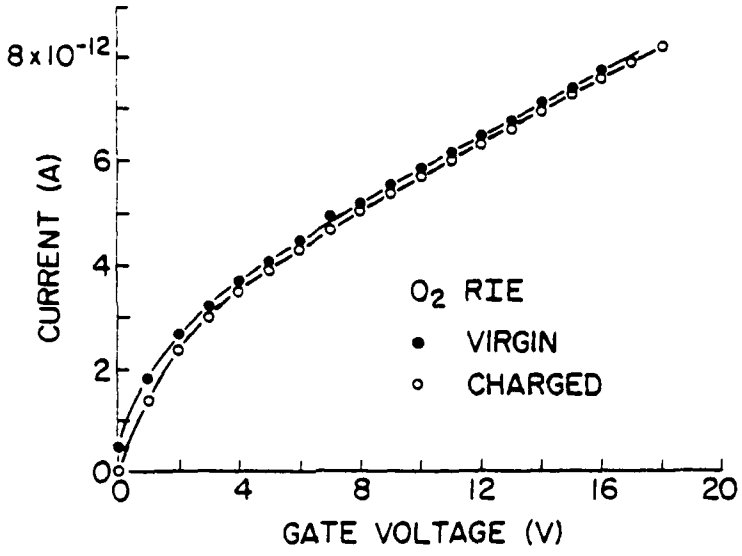

Fig. 12 Magnitude of the current measured in the external circuit for 5-eV light as a function of positive gate voltage (Si injecting) for the same sample before and after charging as in Fig. 11. The average positive photo I-V shift between these curves is $\Delta V_g^+ = 0.6 \pm 0.1$V.

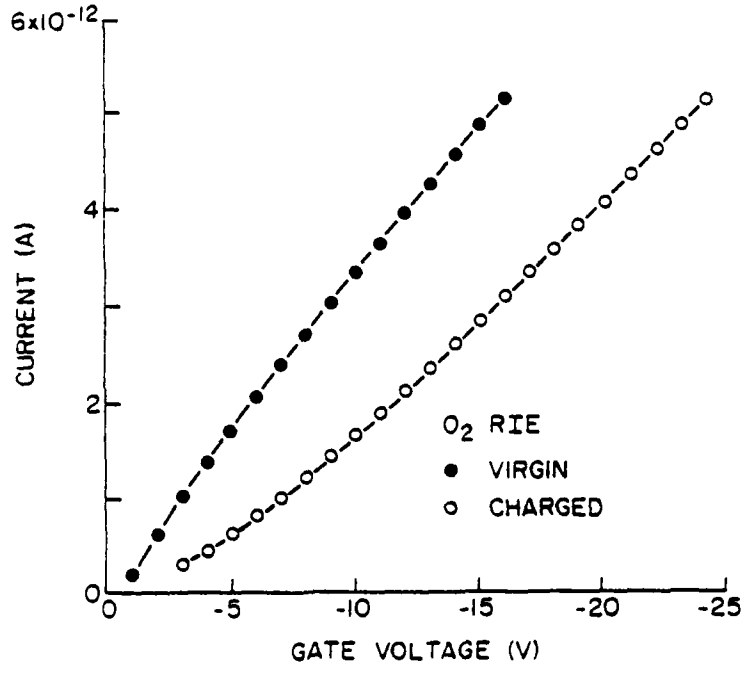

Fig. 13 Magnitude of the current measured in the external circuit for 4.5-eV light as a function of negative gate voltage (Al injecting) for the same sample before and after charging as in Fig. 11. The maximum negative photo I-V shift between these curves is $\Delta V^-_{g_{max}} \geq -8$V. The maximum centroid determined from the photo I-V voltage shifts is 10 ± 1.5 nm.

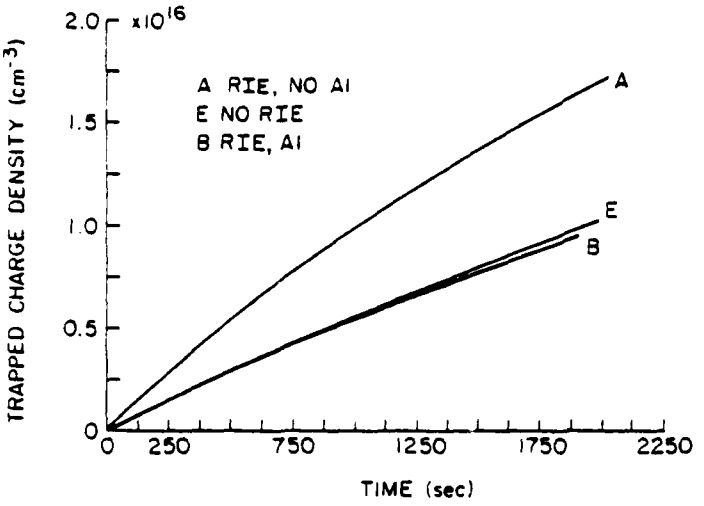

Fig. 14 Volume trapped charge density as a function of avalanche injection time for oxides exposed to RIE with and without an aluminum etch mask. Constant avalanche current = 8×10^{-9} amps.

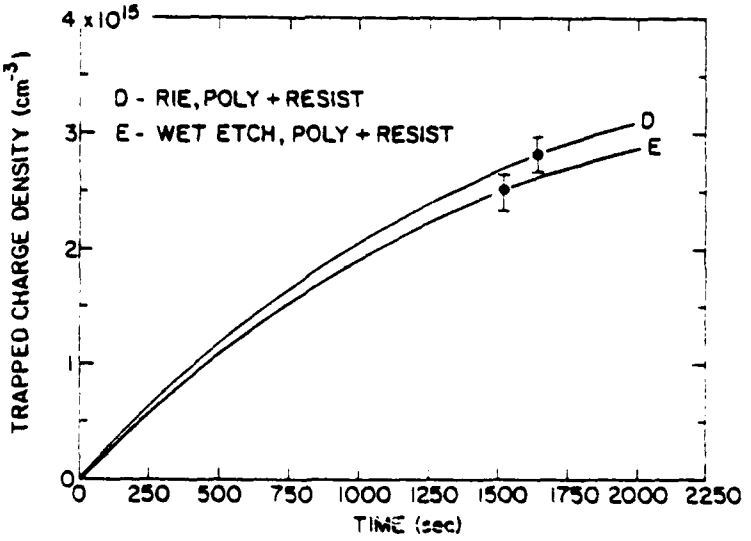

Fig. 15 Volume trapped charge density as a function of avalanche injection time for oxide after RIE of polysilicon electrode. Sample in which polysilicon was wet etched serves as a control. Constant avalanche current = 8×10^{-9} amps.

Effect of Forming Gas Anneal on Al-SiO_2 Internal Photoemission Characteristics

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ABSTRACT

Internal photoemission characteristics from the Al-SiO_2 interface are markedly affected by a 400°C 20 min. forming gas (90% N_2 and 10% H_2) anneal. The barrier height is raised by about 0.25 eV and the electric field dependence of the photocurrent is increased.

Introduction

Recently, several articles have discussed the reaction of Al contacts to SiO_2 in terms of an energy barrier modification at the SiO_2-Al interface. Osburn et al. from dark current measurements [1], Hartstein et al. from photon-assisted tunneling measurements [2], and most recently Hickmott from capacitance-voltage measurements [3] all noticed that post-metallization annealing in either nitrogen or forming gas (90% nitrogen and 10% hydrogen) increased the energy barrier by a few tenths of an electron volt. In this communication, internal photoemission has been used to directly measure the Al-SiO_2 energy barrier heights and study their dependence on the applied electric field. It will be shown here that not only the energy barrier height, but also its electric field dependence is sensitive to post-metallization annealing. It will be demonstrated that ideal Schottky barrier lowering [4] is observed to the highest fields used in this study (~ 5 MV/cm) on samples where the Al-SiO_2 interface has not undergone a forming gas post-metallization anneal. This is contrary to the earlier data of Mead et al. [5] who etched off 25 Å from the surface of their SiO_2 layers grown at 1200°C in O_2 to get a final 550 Å oxide thickness using an HF solution prior to thin Al (150 Å) gate electrode metallization which subsequently was also not annealed. This procedure was not used in our study. Mead et al. described the deviation from ideal Schottky barrier lowering, which they observed, to be due to field penetration into the Al electrode [6]. However, it is more probable that the differences between our data and that of Mead et al. is due to the sensitivity of the Al-SiO_2 interface to sample preparation.

Sample Preparation

Samples were prepared on <100> 0.5 Ω-cm p-type substrates. A 300 Å thick SiO_2 layer was grown at 1000°C in dry O_2, followed by a N_2 anneal, at the same temperature. Aluminum gate electrodes, 30 mil in diameter and 120 Å thick, were then evaporated through

a mask. Subsequently some wafers were annealed in forming gas at 400°C for 20 minutes while others which were unannealed were used as controls.

Experimental Details

For the photocurrent measurements, a 900 W Xenon lamp with a Bausch and Lomb 500-mm grating monochromator set for a 5 nm bandpass and blazed at 300 nm was used to generate the source of photons. The image of the monochromator exit slit always completely covered the circular sample electrode area (.005 cm^2). This monochromator was equipped with a quartz collimating system at the entrance slit and a quartz achromatic focusing system at the exit slit. Cut-off filters were used to remove second- and higher-order light wavelengths. A Keithley model 417 fast picoammeter was used to measure the photocurrents.

The voltages applied to the MOS structures were supplied by stable mercury batteries. The light intensity incident on the sample surface was measured using chopped light techniques. For these measurements, the light was chopped with a 13-Hz Bulova light chopper and sensed using a Reeder thermopile with a CaF_2 window. The thermopile signal was applied to a PAR (Princeton Applied Research) 190 low noise transformer before being detected by a PAR 124 lock-in amplifier.

The oxide was thin enough that optical interference effects could be neglected, and the photocurrent readings were normalized to the incident photon flux. In addition to the photocurrent measurement, capacitance as a function of gate voltage (C-V), and dark current as a function of ramped gate voltage (ramp I-V) measurements were performed.

Experimental Results

Photocurrent measurements were made with the Al under negative voltage bias as a function of applied voltage and photon energy. Care was taken to avoid drift in the character-

istics caused by electron trapping by using low light intensities (photocurrents $< 10^{-8}$ A/cm^2 and low applied fields < 5 MV/cm).

The drift of the photocurrent (monitored at 6 V and 275 nm) was less than 5% during the entire experiment. The C-V curves measured before and after the experiment showed less than 20 mV shifts for the forming gas annealed samples and less than 80 mV shifts for the unannealed samples. The photocurrents were normalized as described above. In calculating the average electric field, a contact potential difference of 0.9 V was assumed. Fowler plots [(photo yield)$^{1/2}$ as a function of photon energy] at various fields are shown in Figs. 1 and 2. Although some workers (e.g. ref. 5,6) have found a cube root plot to give better straight lines, our data fitted the square root plot much better. The curves were least-squares fitted over their linear sections, and the barrier height was derived from the extrapolation to the energy axis. Barrier heights as a function of the average electric field are shown in Fig. 3.

Discussion

As Fig. 3 clearly shows, the barrier height Φ_B and its field dependence are strongly modified by the forming gas post metallization anneal. The non-annealed sample gives a zero field extrapolated barrier height Φ_{BO} of 3.2 eV in agreement with the literature, and its field dependence closely fits the image force barrier lowering model with a high frequency dielectric constant of 2.15. For the theoretical relationship in Fig. 3, q is the magnitude of the charge on an electron, ε_i is the high frequency permittivity of SiO_2, and $\mathcal{E}$ is the average applied electric field. The forming gas annealed sample gives a barrier height of 3.5 eV with a stronger field dependence. The increase in barrier height is consistent with the C-V data, which showed a positive flatband voltage shift of 0.25-0.30 V for the forming gas annealed samples compared to the unannealed controls. The enhanced field dependence in the forming gas annealed sample could indicate that the barrier shape as well as the barrier height has been

modified [6]. To further highlight this point the slope of the Fowler plot as a function of the average applied electric field is shown in Fig. 4a and 4b. According to the simplified theory the photo yield (Y) is given by

$$Y \propto e^{-x_o/\lambda} (h\nu - \Phi_{BO} + \Delta\Phi)^2 \quad (1)$$

where x_o ($\mathscr{E}$) is the distance to the potential maximum according to the image force theory, λ is the interface scattering length parameter [7], $h\nu$ is the incident photon energy, and $\Delta\Phi$ ($\mathscr{E}$) is the energy barrier lowering ($\Delta\Phi = [q \div (4\pi\epsilon_i)]^{\frac{1}{2}} \mathscr{E}^{\frac{1}{2}}$). The slope of the Fowler plot is just the exponential scattering term in Eq. 1, and therefore is very sensitive to the interface scattering parameter and the initial barrier shape. We see from Fig. 4 that the unannealed sample follows the predicted dependence with an interface scattering length parameter of about 25 Å. The forming-gas annealed sample deviates from this, especially at high fields. This upward turn at high fields in the characteristic of Fig. 4 on the annealed structure as compared to the unannealed structure was observed on all samples tested. This data suggests that the forming gas anneal modifies the energy band structure near the interface and that the transition region may be considerable in extent (~ 25 Å). This is in contrast to the unannealed sample, where, in agreement with ref. 6, a sharp interface (~ 5 Å transition region) is observed. The barrier raising is consistent with a larger energy bandgap, a negative charged species, or a dipole layer near the interface. The magnitude of the barrier raising is consistent with Hickmott's data [3].

Acknowledgements

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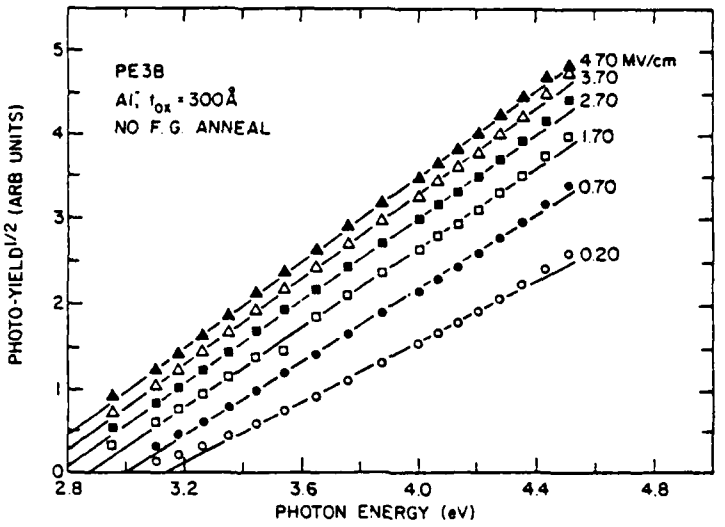

Fig. 1: Square root of the photo-yield as a function of photon energy for various electric fields under negative gate voltage bias on a sample which had no forming gas anneal.

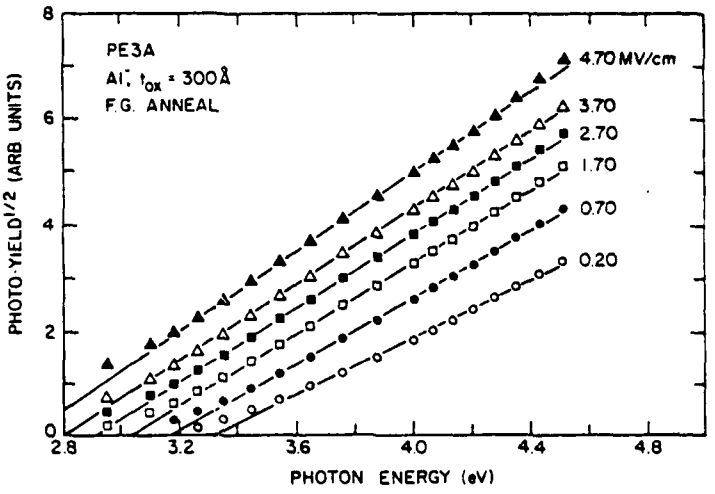

Fig. 2: Square root of the photo-yield as a function of photon energy for various electric fields under negative gate voltage bias on a sample which had a forming gas anneal.

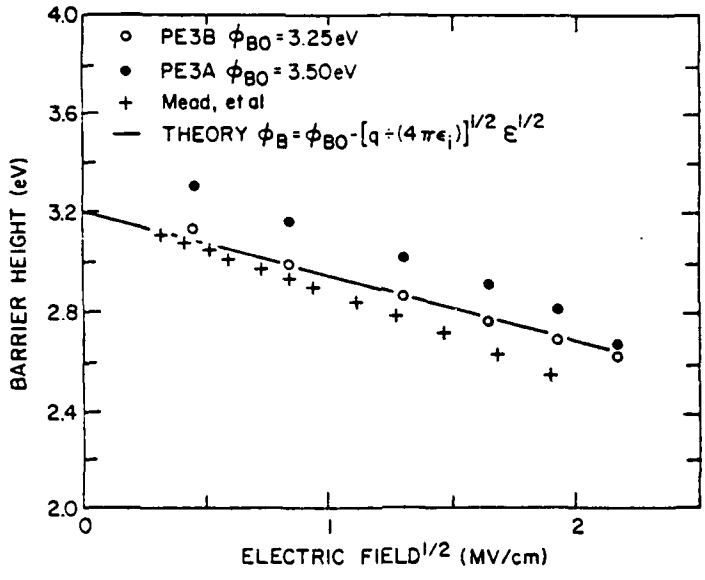

Fig. 3: Comparison of the Al-SiO_2 interfacial energy barrier height as a function of the square root of the electric field for negative gate voltage bias deduced from the experimental data of Figs. 1 and 2. Data from Mead et al. (Reference 5) and the theoretical relationship are also plotted for comparison.

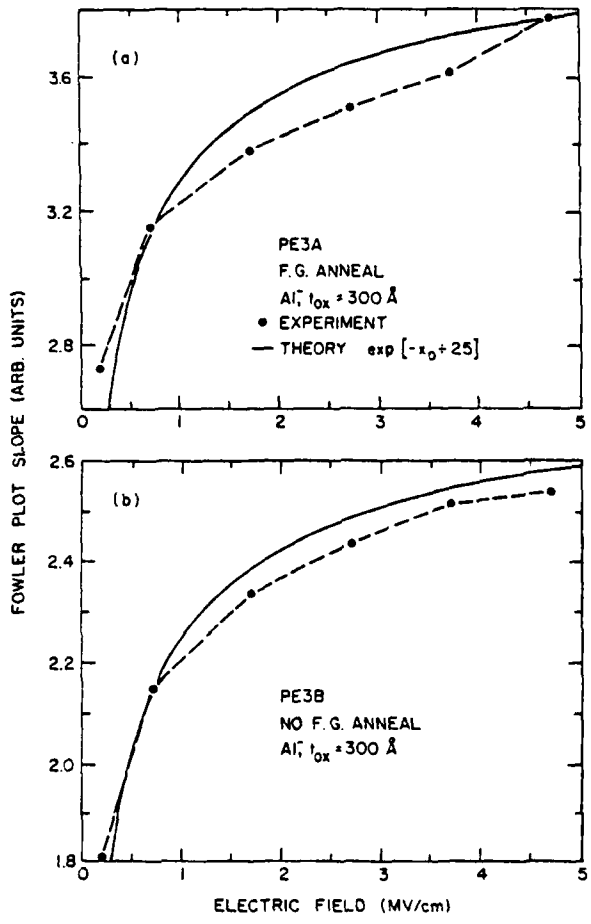

Fig. 4: Comparison of the slopes deduced from the Fowler plots in Figs. 1 and 2 as a function of the electric field for negative gate voltage bias. The theoretical relationship is also plotted for comparison.

SILICON OXIDATION STUDIES: MEASUREMENT OF THE DIFFUSION OF OXIDANT IN SiO_2 FILMS

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ABSTRACT

A method for the measurement of the diffusion of oxidant through a growing SiO_2 film is presented. The procedure is based on so called lag-time diffusion methods in which the time to achieve steady state oxidation is measured using in-situ ellipsometry. Two different modes of oxidant transport were observed over the range of temperatures investigated (600°C - 1000°C). At temperatures of 900°C and below, no lag-time was observed; and steady state oxidation was seen at the outset of oxidation. At 1000°C, a lag-time was measured which yielded a value for the diffusion constant, $D = 2.3 \times 10^{-13}$ cm^2/sec for dry O_2 and this value decreased to 2.4×10^{-12} cm^2/sec for 1000 ppm H_2 in O_2. This study provides clear evidence for different dominant modes of oxidation at higher and lower oxidation temperatures.

Introduction

The thermal oxidation of silicon is generally believed to proceed by a process that encompasses a steady state of both diffusion of oxidant through an SiO_2 film and reaction of this oxidant with Si at the Si-SiO_2 interface. This notion of the mechanism of oxidation of silicon is primarily due to the success of the linear - parabolic oxidation model[1] in correlating the silicon oxidation data (see for example early reports in Refs. 2 and 3). Virtually every worker in this field has reported parabolic-like oxidation behavior i.e., a decrease in the thermal oxidation rate of silicon with time. This plus the several studies that show that oxidant rather than silicon is the primary transported species[4-6] support the diffusion-reaction model. The statistical treatment of copious oxidation data demonstrate reasonable predictability (less than 10% error) of this model[7-9]. However, this model is largely phenomenological and therefore contributes only little to the understanding of the details of the oxidation mechanism.

The present study is aimed towards a better understanding of the details of the transport of oxidant across the SiO_2 film. To probe this transport process, the well known lag-time diffusion technique[10,11] for thin membranes has been adapted to measure the oxidant transport during oxidation. Basically, the oxidation process is followed using in-situ ellipsometry. The analytical technique assumes Fickian diffusion of oxidant through the growing oxide film i.e., transport in response to a concentration gradient and can therefore be used to test for true diffusion as the dominant mode of oxidant transport.

In the literature, there exists diffusion data for oxygen in fused silica[12-15]. These studies report divergent values for both the diffusion constant, D (several orders of magnitude) and the activation energy for diffusion (a factor of more than three). Diffusion data for oxygen in thin films of SiO_2 has to my knowledge not been reported. Since it is known[16] that the precise method of preparation (temperature, impurities etc.) of amorphous materials determines many of the physical properties of the material, it is likely that part of the spread in the existing data is due to differing samples. Therefore, in order to understand the oxidation of Si

to form SiO_2 films, it is important that the measurement of diffusion be done for thin SiO_2 films.

The present study will present the lag-time method using ellipsometry. Secondly, the method will be used to obtain data and then an interpretation will be presented. The application of this lag-time technique has enabled the measurement of D associated with oxygen transport in SiO_2 at 1000°C and has shown that a lag-time is not observed at 900°C and below. In addition, it was discovered that linear parabolic kinetics obtain at the outset of oxidation for temperatures of 900°C and below even for films 100 nm thick. These experimental results lead to considering alternatives to pure Fickian diffusion as the dominant mode of transport of oxygen through SiO_2 films at the lower oxidation temperatures.

Experimental Procedures

Sample Preparation: The experimental technique utilizes SiO_2 films grown by the oxidation of single crystal silicon. The starting silicon wafers were commercially available chem-mechanically polished 2Ω-cm p-type with (100) orientation. The silicon was cleaned by a previously outlined procedure[7] and the starting SiO_2 films were prepared via thermal oxidation in dry O_2 at 1000°C.

Ellipsometry: The automated ellipsometer used for the present study as well as optical constants and procedures were previously described[7,17]. The ellipsometer can measure oxide growth while the sample is under oxidation conditions. A typical experiment is started by placing a previously grown SiO_2 film of about 10^4Å on a Si wafer in the oxidation furnace of the automated ellipsometer. The sample is then heated at 1000°C in either N_2 or Ar for about 20 hours. The film thickness is periodically measured to check the quality of the N_2 or Ar and to provide baseline initial oxide thickness data. At some arbitrary time after outgasing, the temperature is adjusted and equilibrated at the desired value and the ambient is switched to oxygen. Before and after this ambient change, SiO_2 thickness is measured continuously.

The experiment is usually continued for more than 40 hours after O_2 is turned on to insure that steady state oxidation is achieved.

In order to insure that any change noticed by ellipsometry is due to a change in SiO_2 thickness and not perhaps a change in optical absorption, a separate experiment was performed. A disc of optical quality fused silica of about 0.64 cm thick and 2 cm in diameter polished on one face and purposely frosted on the other face was placed in the ellipsometer furnace. The polished surface was monitored by ellipsometry and Δ and Ψ data was taken at various temperatures between 600 and 1000°C before and after switching the ambients. No change is the optical constants of the fused silica was observed. Therefore, any change observed for the thick SiO_2 films on Si would be attributed to a real change in the SiO_2 film thickness. As will be shown below, this lag-time experiment performed at or below 900°C yielded initial oxidation rates equal to final rates i.e., no lag-time. Without the experiment above, this observation could possibly be trivially explained by a difference in the optical constants of the oxide in N_2 or O_2 when the ambient is switched. On the other hand, the rapid attainment of steady state oxidation at the lower experimental temperatures has mechanistic implications and this will be covered in the discussion section.

The temperature range 1000°-600°C was explored; higher temperatures could not be attained in the present equipment.

Lag-Time Method

The lag-time method[10,11] is based on the existence of a time delay for the transport of a gas through a membrane that initially has zero concentration of the gas. The time delay is measured from the time the temperature equilibrated membrane contacts the gas (t=o) to the time the gas appears on the other side of the membrane as a steady state flow.

The lag-time analysis due to Daynes[10] and Barrer[11] is herein adapted to the Si-SiO_2-oxygen system. The key equations and boundary conditions are reproduced below with some modification from the published detailed analysis[10,11]. For the Si-SiO_2-oxygen gas system, the boundary conditions are shown in Fig. 1 and the general solution for concentration is:

$$C = C_1 + (C_2 - C_1)\frac{X}{L} + \frac{2}{\pi}\sum_{m=1}^{\infty}\left(\frac{C_2 \cos n\pi - C_1}{n}\right)\left(\sin\frac{n\pi X}{L}\right)\exp\left(\frac{-D n^2\pi^2 t}{L^2}\right)$$

$$+ \frac{4C_o}{\pi}\sum_{m=o}^{\infty}\frac{1}{(2m+1)}\sin\frac{(2m+1)\pi X}{L}\exp\left(\frac{-D(2m+1)^2\pi^2 t}{L^2}\right) \quad (1)$$

Where C is the concentration of oxidant at any time. At the Si-SiO_2 interface, X=O and

$$\left(\frac{\partial C}{\partial X}\right)_{x=o} = \frac{C_2 - C_1}{L} + \frac{2}{L}\sum_{n=1}^{\infty}(C_2\cos n\pi - C_1)\exp\left(\frac{-D n^2\pi^2 t}{L^2}\right)$$

$$+ \frac{4C_o}{L}\sum_{m=o}^{\infty}\exp\left(\frac{-D(2m+1)^2\pi^2 t}{L^2}\right) \quad (2)$$

The rate at which gas, C_g, emerges from a membrane of unit area at X=O is given as:

$$\frac{\partial C_g}{\partial t} = D\left(\frac{\partial C}{\partial X}\right)_{x=o} \quad (3)$$

Now substituting $\left(\frac{\partial C}{\partial X}\right)_{x=o}$ from above and solving for the concentration, C_g, by integration the resultant equation is:

$$C_g = \frac{D(C_2 - C_1)t}{L} + \frac{2L}{\pi^2}\sum_{n=1}^{\infty}\left(\frac{C_2\cos n\pi - C_1}{n^2}\right)\left(1 - \exp\left(\frac{-D n^2\pi^2 t}{L^2}\right)\right)$$

$$+ \frac{4C_o L}{\pi^2}\sum_{m=o}^{\infty}\frac{1}{(2m+1)^2}\left(1 - \exp\left(\frac{-D(2m+1)^2\pi^2 t}{L^2}\right)\right) \quad (4)$$

This concentration will increase towards a steady state as $t \rightarrow \infty$ and C_g approaches the line:

$$C_g = \frac{D}{L}\left[(C_2 - C_1)\,t + \frac{2L^2}{D\pi^2}\sum_{n=1}^{\infty}\left(\frac{C_2\cos n\pi - C_1}{n^2}\right)\right.$$

$$\left. + 4\,\frac{C_o L^2}{\pi^2 D}\sum_{m=o}^{\infty}\frac{1}{(2m+)^2}\right] \tag{5}$$

$$= \frac{D}{L}\left[(C_2 - C_1)\,t - \frac{C_2 L^2}{6D} - \frac{C_1 L^2}{3D} + \frac{C_o L^2}{2D}\right]. \tag{6}$$

The intercept of this line with the time axis yields the lag-time, τ:

$$\tau = \frac{1}{(C_2 - C_1)}\left[\frac{C_2 L^2}{6D} + \frac{C_1 L^2}{3D} - \frac{C_o L^2}{2D}\right]. \tag{7}$$

If the actual experiment commences with no oxidant in the film, $C_o = o$, and if the reaction at the Si-SiO_2 interface is fast relative to transport then $C_1 \approx o$, then the lag-time expression reduces to the equation:

$$\tau = \frac{L^2}{6D} \tag{8}$$

The condition of $C_o = o$ is achieved by a thorough outgas of the sample at 1000°C overnight while the condition $C_1 \approx o$ is consistent with the linear - parabolic model.

The steady state condition is observed by the conformity of the thickness-time data to the linear parabolic rate law:

$$t = AL + BL^2 \tag{9}$$

where t is the oxidation time for a film thickness L, and A and B are the reciprocals of the linear and parabolic rate constants, respectively. For very thin films, there is an offset in the t and L axes to account for the initial regime of oxidation which does not conform to linear - parabolic kinetics. The form of this corrected equation is:

$$t-t_o = A\,(L-L_o) + B\,(L^2-L_o^2) \qquad (10)$$

However, for the present study, films greater than 500 nm (typically 1000 nm) will be used so that L >500 nm while L_o <50 nm and similarly t >> t_o and therefore Eq. 9 can be used. Equation 9 is easily linearized and linear least squares analysis of the t and L data according to L versus t/L yield slope and intercept values that are used to extrapolate to the time axis at the initial oxide thickness value. This intersection yields the τ value used with the average L value in Eq. 8 to obtain D.

To insure that steady state is achieved, oxidation is carried out for more than forty hours. Thickness-time data from the last 10 hours are analyzed as steady state values. However, prior to any data analysis, the overall L, t data is sampled in the first and second hours of oxidation and then after 20, 30 and 40 hours. If the lag-time method is applicable, the oxidation rates should be initially low and then increasing towards steady state. This information provides the basis for the lag-time analysis.

Results and Discussion

In order to assess the range of possible lag-time values, τ values were calculated from the divergent D values of Norton[12] and Williams[13] and the results are shown in Table 1. It is seen that if Norton's values for D are applicable for SiO_2 films, then τ is virtually unmeasurable by the present technique down to 800°C and marginally measurable down to 600°C. However, based on Williams' data, τ can be easily measured at 1000°C and below. Therefore,

if the measured D values for oxidant in the SiO_2 films used for this study are near Norton's[12] values, we would expect to see no lag-time for the higher temperatures while if Williams'[13] D values obtain, a lag-time would be observed for all temperatures, and for both sets of D values the τ values would be larger for the lower temperatures. The experimental data which consists of thickness-time measurements on films with starting thickness of about 10^4Å was first surveyed to determine whether lag-times were observed. As previously stated, this was done by comparing the rates of oxidation at the beginning of the experiment to rates at the end. Table 2 lists these rates as rounded off numbers for the 1st, 2nd, 20th, 30th, 40th, hours of the experiment. It is clearly seen that only at 1000°C is true lag-time behavior observed i.e., the rate of oxidation increases to a steady-state value. For the lower temperatures, the initial rates are at least equal to final rates. There is some data that shows a slight trend toward the initial rate being larger than final rates. However, this type of behavior is anticipated based on linear parabolic kinetics. Representative SiO_2 thickness versus oxidation time data is shown as Figs. 2a and 3a for 1000°C and 800°C respectively. The 1000°C data has a smaller initial slope than for long times and the opposite is true at 800°C.

Figures 2b and 3b show plots of L versus t/L at 1000°C and 800°C, respectively. It is clear that the 800°C data is well represented by the linear-parabolic model and this was also typical for the 900°C, 700°C and 600°C data. The 1000°C data shows the expected deviation for shorter times which is indicative of the existence of a lag-time. The 1000°C data was analyzed by linear least squares fitting of L versus t/L at long times and then finding the intersection of this line with the t/L axis. The intersection is τ/L_o where L_o is the starting oxide thickness. τ is then used in Eq. 8 to calculate a value for the diffusion constant, D = 2.3×10^{-13} cm^2/sec at 1000°C in dry O_2. This value is about one order of magnitude larger than Williams'[13] value at 1000°C. The value for the lag-time is τ = 8490 sec. It is interesting to compare this value for τ with the value of 8804 sec calculated from the formula derived by considering the approach to steady state flow through a plane sheet by Crank[18]:

$$\frac{D\tau}{L^2} \approx 0.45 \tag{11}$$

From the relationship between permeability, P, diffusivity, D, and solubility, S:

$$S = \frac{PL}{D} \tag{12}$$

which applies when Henry's law is obeyed, the solubility can be calculated. The permeability is the steady state oxidant flux which is calculated from the rate of oxidation. At 1000°C the permeability is about $P = 2.7 \times 10^{-12}$ O_2's cm^{-2} sec^{-1} for 1 atm O_2 pressure. This yields a value for solubility of $S = 1.2 \times 10^{21}$ cm^{-3} which is considerably higher than Deal's[2] value of 5.2×10^{16} cm^{-3} calculated using the relationship:

$$S = \frac{k_{PAR} \cdot 2.25 \times 10^{22}}{2D}, \tag{13}$$

and Norton's[12] value for D, where k_{PAR} is the parabolic rate constant. The reason for the large difference in S values in the present study and Deal's study[2] is due primarily to differences in D. Using the value for D obtained in this study and Deal's k_{PAR}[2], S is calculated to be 1.6×10^{21} cm^{-3}.

To determine the effect of H_2O on D, 1000 ppm was added to dry O_2 by a previously outlined procedure[19]. The data at 1000°C showed a lag-time, and a value of $D = 2.4 \times 10^{-12}$ cm^2/sec or about a tenfold increase in D with 1000 ppm H_2O was obtained. From previous studies of the affect of H_2O on the rate of Si oxidation[19], we reported less than a twofold increase in rate with 1000 ppm H_2O in O_2. From Eq. 12, if D increases by a factor of 10 and P by a factor of 2 then the solubility of oxidant in the presence of 1000 ppm H_2O must actually decrease by a factor of five. This result may indicate that although trace amounts of

H_2O enhance diffusion of oxidant so that the rate of oxidation increases, the H_2O ties up many active sites in SiO_2 thereby lowering the solubility for O_2.

In terms of the mechanism of oxidation, the present results demonstrate the existence of a change in the dominant mechanism for oxidant transport near 1000°C. Above this temperature, the transport can be considered Fickian with undissociated oxygen as the likely transported species. This latter contention is based on the observation that Henry's law is obeyed at high temperatures[2]. The question of whether any transported species are charged is not addressed in this study. Further evidence for the change in predominant mechanism of oxidation was obtained from an earlier study[20] in which considerable curvature in Arrhenius plots involving both linear and parabolic rate constants was reported. In that study[20], the higher temperatures yielded a lower activation energy for k_p in agreement with earlier studies[2] that also emphasized oxidation temperatures above 1000°C. The lower temperatures yielded activation energies for k_p more than 50% larger[20]. The mechanism for oxidation below 1000°C is likely to involve a superposition of Fickian diffusion which is predominant at higher temperatures with at least one additional mode of transport. Excluding models which involve charged species, two kinds of mechanisms come to mind which would explain the rapid attainment of steady state oxidation. One model considers the migration of atomic oxygen from network position to network position. Such a mechanism does not require long distance migration of oxygen to initiate oxidation. Rather, when one atom of oxygen is taken into the network at the gas - SiO_2 interface, an atom then becomes available at the Si-SiO_2 interface for oxidation. This process takes place on a time scale of atomic vibrations and would therefore explain the rapid attainment of steady state behavior. However, the recent tracer studies of Rosencher et al[21] and Pfeffer and Ohring[22] demonstrate that oxygen is transported across the oxide with little or no interaction with the network. Another possibility is to consider the flow of oxidant in micropores. If micropores exist in sufficient numbers and if the pores penetrate to the Si-SiO_2 interface then very slow diffusion at low temperatures may be short circuited by the flow of oxidant in micropores. Previous studies on

thin SiO_2 films yielded some indirect evidence for the existence of micropores in SiO_2 films[23] and recent transmission electron microscopy studies by Gibson and Dong[24] have shown micropores of about 10Å to exist in dry O_2 grown SiO_2 films. Further work on a micropore model is necessary and in progress but it is interesting to note that if Knudsen - Poiseuille flow is considered in micropores[25] in steady state with linear surface kinetics a linear - parabolic type rate law can be derived. The fact that lower oxidation temperatures yield higher density SiO_2[26,27] probably also contributes to a decrease in the importance of simple diffusion and perhaps renders a different transport mechanism dominant at lower oxidation temperatures.

Meek[28] has attempted to explain the large discrepancy between Norton[12] and Williams[13] measurements of D for oxygen in fused silica based on the differences in the experimental techniques viz., Norton measures chemical diffusion based on a lag-time while Williams measures the transport of a radioisotope. According to Meek's interpretation, Williams measured value of D is necessarily smaller than Norton's due to the fraction of time the radioisotope spends in exchanging with the network rather than in the interstices of SiO_2. Recently, however, two definitive studies[22,29] have appeared in the literature which show that the transported oxygen does not exchange to any measurable extent with the SiO_2 network. Therefore, it is now clear that Meeks argument does not apply and the large differences in the D data can be explained either trivially by experimental errors or by real differences in the SiO_2 itself. It is quite clear that both Pfeffer and Ohring[22] and Rigot et al[29] find large differences in the behavior of oxygen in SiO_2 when H_2O is present and it is not unreasonable to speculate that impurities and perhaps even fictive temperature and other preparation conditions lead to the large reported differences in D values.

In summary, a method to measure diffusion of oxidant in growing SiO_2 films has been developed. This method is based on Fickian diffusion through a membrane and therefore can be used to test for diffusion conditions.

Diffusion of O_2 in SiO_2 as the mode of oxidant transport has been found as the dominant mechanism at 1000°C and a value of $D = 2.3 \times 10^{-13}$ cm^2/sec has been measured. This value decreases by an order of magnitude with 1000 ppm H_2O in the O_2. At lower temperatures, a different mode of oxidant transport is dominant. This mode is characterized by the instantaneous achievement of steady state linear - parabolic oxidation kinetics.

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TABLE I

T(°C)

	1000	900	800	700	600
D (cm^2/sec) From Norton (12)	$6x10^{-9}$	$3x10^{-9}$	$9x10^{-10}$	$3x10^{-10}$	$5x10^{-11}$
τ (sec) for 1μ SiO_2	.3	.6	2	7	32
D (cm^2/sec) From Williams (13)	$2x10^{-14}$	$9x10^{-15}$	$3x10^{-15}$	$7x10^{-16}$	$1x10^{-16}$
τ (sec) for 1μ SiO_2	$8x10^4$	$2x10^5$	$6x10^5$	$2x10^6$	$2x10^7$

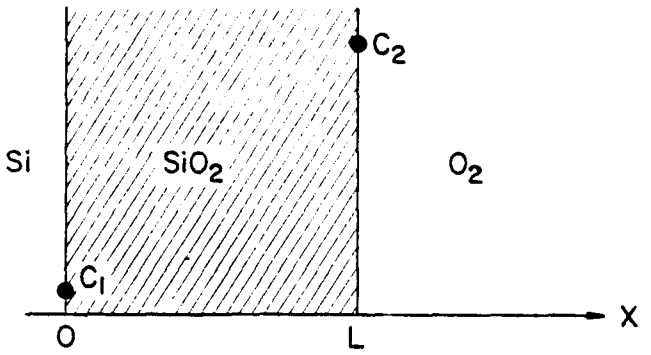
Table 1. Literature Values of D and Calculated Values for the Lag-Time, τ.

TABLE II

OXIDATION RATES (Å/hr)

T(°C)	1st	2nd	20th	30th	40th
1000	33	37	38	44	44
900	20	18	20	20	21
800	10	9	9	9	8
700	2	2	2	3	2
600	.7	.5	.4	.3	.3

Table 2. Comparison of Initial and Final Rates of Oxidation



$C = C_1$ AT $X = 0$ FOR ALL t

$C = C_2$ AT $X = L$

$C = C_0$ FOR $0 < X < L$ AT $t = 0$

Fig. 1. Pictorial representation of Si-SiO_2-O_2 system with boundary conditions

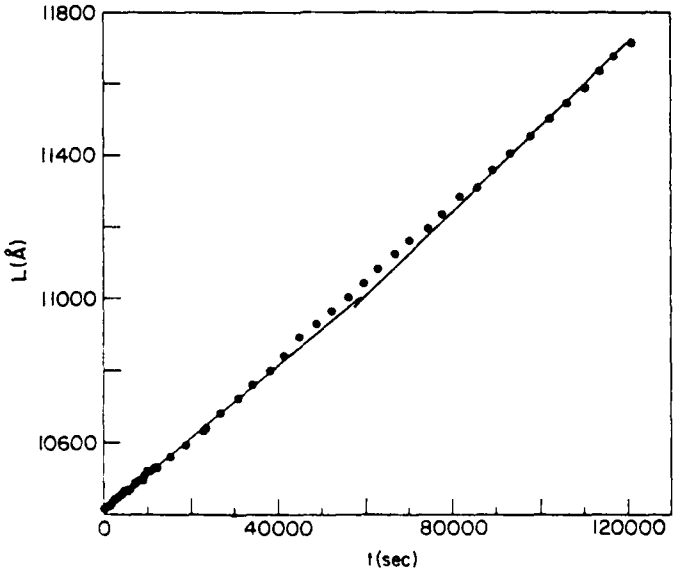


FIGURE 2A

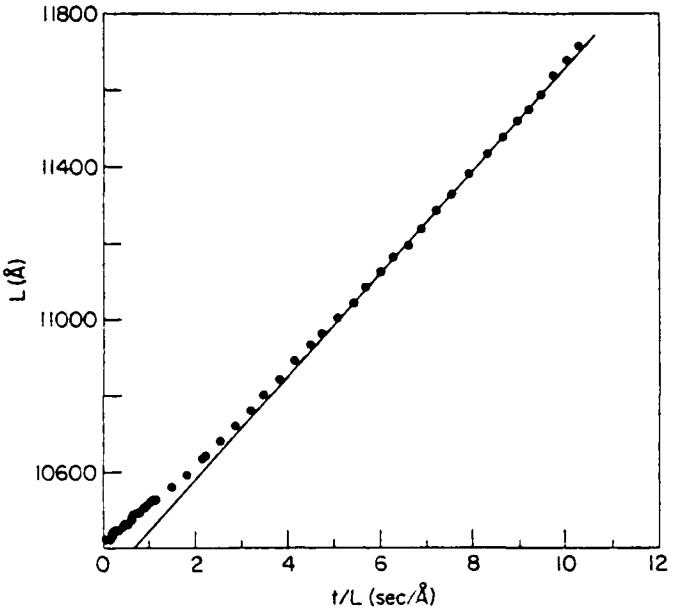


FIGURE 2B

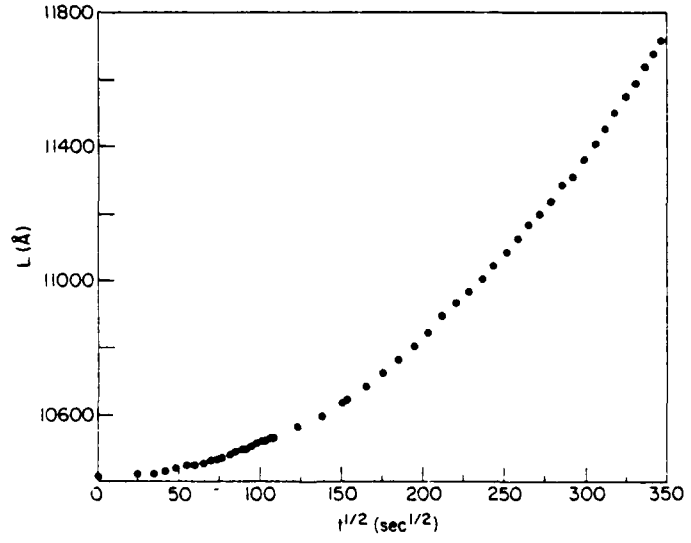


FIGURE 2C

Fig. 2. Thickness, L, and time, t, oxidation data for dry O_2 at 1000°C: a) as L vs. t; b) L vs. t/L and c) L vs. $t^{\frac{1}{2}}$.

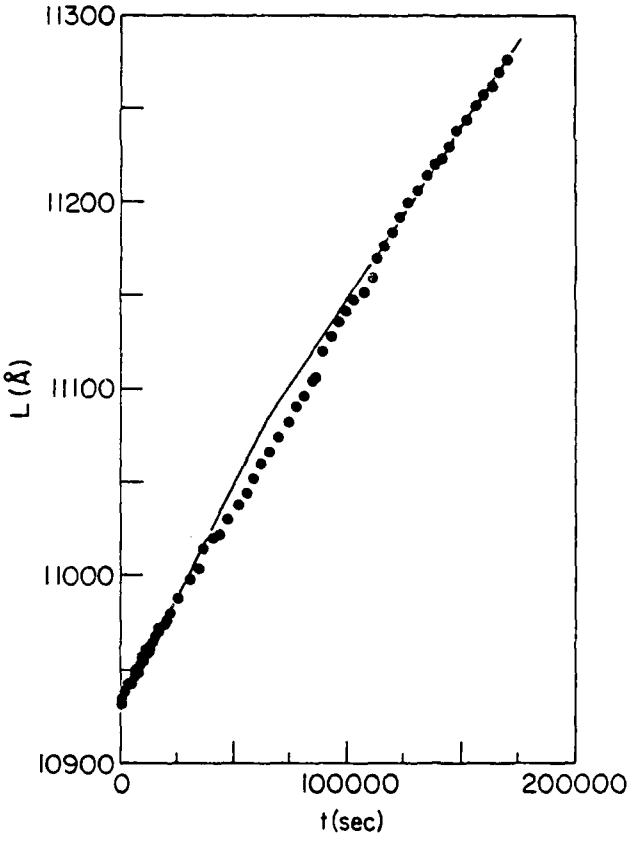


FIGURE 3A

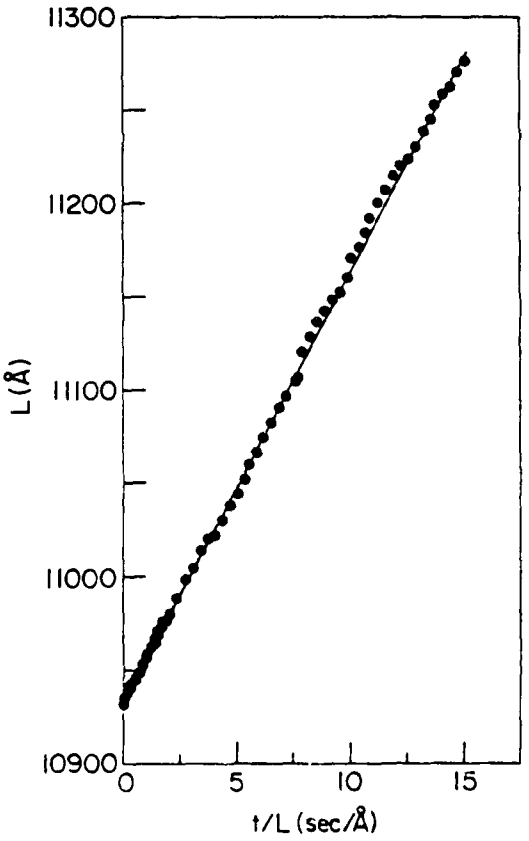


FIGURE 3B

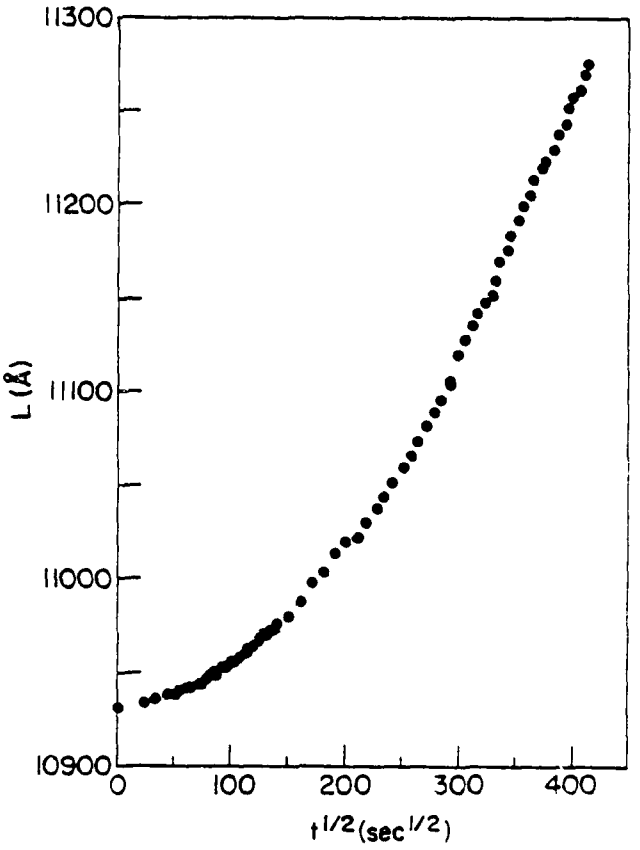


FIGURE 3C

Fig. 3. Thickness, L, and time, t, oxidation data for dry O_2 at 800°C: a) as L vs. t; b) L vs. t/L and c) L vs. $t^{\frac{1}{2}}$.

ANL